Recognized as an
American National Standard (ANSI)

IEEE Std C62.37-1996

IEEE Standard Test Specification for Thyristor Diode Surge Protective Devices

Sponsor

Surge Protective Devices Committee
of the
IEEE Power Engineering Society

Approved 23 October 1996

IEEE Standards Board

Approved 1 April 1997

American National Standards Institute

Abstract: This standard applies to two or three terminal, four or five layer, thyristor surge protection devices (SPDs) for application on systems with voltages equal to or less than 1000 V rms or 1200 V dc.

Keywords: test specification, thyristor surge protective devices

---

The Institute of Electrical and Electronics Engineers, Inc.
345 East 47th Street, New York, NY 10017-2394, USA

ISBN 1-55937-897-2

IEEE Standards documents are developed within the IEEE Societies and the Standards Coordinating Committees of the IEEE Standards Board. Members of the committees serve voluntarily and without compensation. They are not necessarily members of the Institute. The standards developed within IEEE represent a consensus of the broad expertise on the subject within the Institute as well as those activities outside of IEEE that have expressed an interest in participating in the development of the standard.

Use of an IEEE Standard is wholly voluntary. The existence of an IEEE Standard does not imply that there are no other ways to produce, test, measure, purchase, market, or provide other goods and services related to the scope of the IEEE Standard. Furthermore, the viewpoint expressed at the time a standard is approved and issued is subject to change brought about through developments in the state of the art and comments received from users of the standard. Every IEEE Standard is subjected to review at least every five years for revision or reaffirmation. When a document is more than five years old and has not been reaffirmed, it is reasonable to conclude that its contents, although still of some value, do not wholly reflect the present state of the art. Users are cautioned to check to determine that they have the latest edition of any IEEE Standard.

Comments for revision of IEEE Standards are welcome from any interested party, regardless of membership affiliation with IEEE. Suggestions for changes in documents should be in the form of a proposed change of text, together with appropriate supporting comments.

Interpretations: Occasionally questions may arise regarding the meaning of portions of standards as they relate to specific applications. When the need for interpretations is brought to the attention of IEEE, the Institute will initiate action to prepare appropriate responses. Since IEEE Standards represent a consensus of all concerned interests, it is important to ensure that any interpretation has also received the concurrence of a balance of interests. For this reason, IEEE and the members of its societies and Standards Coordinating Committees are not able to provide an instant response to interpretation requests except in those cases where the matter has previously received formal consideration.

Comments on standards and requests for interpretations should be addressed to:

Secretary, IEEE Standards Board
445 Hoes Lane
P.O. Box 1331
Piscataway, NJ 08855-1331
USA

Note: Attention is called to the possibility that implementation of this standard may require use of subject matter covered by patent rights. By publication of this standard, no position is taken with respect to the existence or validity of any patent rights in connection therewith. The IEEE shall not be responsible for identifying all patents for which a license may be required by an IEEE standard or for conducting inquiries into the legal validity or scope of those patents that are brought to its attention.

Introduction

(This introduction is not part of IEEE Std C62.37-1996, IEEE Standard Test Specification for Thyristor Diode Surge Protective Devices.)

This test specification has been developed to enable the unified definition, test, and evaluation of thyristor type surge protective device parameters. A thyristor surge protective device limits overvoltages by switching on and providing a low impedance path to divert the current resulting from the overvoltage. Fixed voltage thyristor surge protective devices have their limiting voltage determined by the manufacturing process. Gated thyristor surge protective devices may have their limiting voltage determined by the reference potential applied to the gate. By connecting the gate in series with the circuit conductors, overcurrent conditions can also initiate device switch on and current diversion.

Thyristor devices have been used since the early 70s to protect telecommunications equipment against induced and conducted overvoltages caused by lightning and ac systems. These devices were specially engineered to provide the required protection function. The device main features were an extended breakdown region and an abnormally high value of holding current. As a result, many of the conventional thyristor terms and test methods were inadequate for these thyristor surge protective devices. Being a new device variant, many existing surge protective device manufacturers and users applied terms and tests used for gas-discharge tubes or avalanche junction semiconductor surge protective devices. Compared to these established devices, the thyristor surge protective device has different circuit sensitivities and this resulted in poor parameter correlation between users and suppliers.

There was a need for a comprehensive thyristor surge protective device test standard that defined terms, detailed appropriate test circuits, and measurement conditions. The Low-Voltage Solid-State Surge Protective Devices Working Group 3.6.2 of the IEEE Surge Protection Devices Committee under took the task of preparing such a standard. The Working Group was formed from experts and interested parties drawn from producers, users, service providers, standards authorities, equipment manufacturers, test equipment manufacturers, and laboratories.

The Accredited Standards Committee on Surge Arresters, C62, at the time of ballot, had the following members:

Joseph L. Koepfinger, *Chair* **John A. Gauthier,** *Secretary*

Organization Represented	*Name of Representative*
Association of American Railroads	Wayne Etter
Bonneville Power Administration	G. E. Lee
Canadian Standards Association	D. M. Smith
Electric Light and Power	J. W. Wilson R. A. Jones W. A. Maguire G. N. Miller *(Alt.)* T. A. Wolfe
Institute of Electrical and Electronics Engineers	J. L. Koepfinger J. J. Burke G. L. Gaibrois W. H. Kapp Richard Odenberg Keith Stump Edgar Taylor *(Alt.)*
Members-at-Large	J. Osterhout B. Pensar Steven G. Whisenant
National Electrical Manufacturers Association	Dennis W. Lenk Larry Bock *(Alt.)* Andi Haa Paul Jeffries Hans Steinhoff Jonathan J. Woodworth Dennis W. Lenk
National Institute for Science and Technology	F. D. Martzloff
Rural Electrification Administration	(vacant)
Underwriters Laboratories	George Mauro
Individuals	Joseph Osterhout B. Pensar Steven G. Whisenant

At the time this standard was completed, the Low-Voltage Solid-State Surge Protective Devices Working Group 3.6.2 had the following membership:

Richard Odenberg, *Chair* **Michael J. Maytum,** *Secretary*

John Brittain	David W. Hutchins	John A. Siemon
Nisar Chaurdhry	Wilhelm Kapp	Donald B. Turner
Curtis A. Domsch	Benny H. Lee	Dee Unterweger
Ernie Gallo	William J. Shannon	Jonathan Woodworth
Jim Harrison		Don Worden

Other individuals who have contributed review and comments are:

Rickard Bentinger
Stan Bonnesen
Chrysanthos Chrysanthou
Barry Epstein
C.A. Francis, II
Robert Fried
Allan F. Holland
Joe L. Koepfinger
Ed H. Marrow, Jr.
Albert A. Martin
Kurt A. Meindorfer
George Templeton

The following persons were on the balloting committee:

Chrys Chrysanthou
David W. Hutchins
David W. Jackson
Wilhelm Kapp
Joseph L. Koepfinger
Francois D. Martzloff
Richard Odenberg
Joseph C. Osterhout
Edgar R. Taylor
Arnold Vitols
J. W. Wilson
Donald M. Worden

When the IEEE Standards Board approved this standard on 23 October 1996, it had the following membership:

Donald C. Loughry, *Chair* **Richard J. Holleman,** *Vice Chair*
Andrew G. Salem, *Secretary*

Gilles A. Baril
Clyde R. Camp
Joseph A. Cannatelli
Stephen L. Diamond
Harold E. Epstein
Donald C. Fleckenstein
Jay Forster*
Donald N. Heirman
Ben C. Johnson
E. G. "Al" Kiener
Joseph L. Koepfinger*
Stephen R. Lambert
Lawrence V. McCall
L. Bruce McClung
Marco W. Migliaro
Mary Lou Padgett
John W. Pope
Jose R. Ramos
Arthur K. Reilly
Ronald H. Reimer
Gary S. Robinson
Ingo Rüsch
John S. Ryan
Chee Kiow Tan
Leonard L. Tripp
Howard L. Wolfman

*Member Emeritus

Also included are the following nonvoting IEEE Standards Board liaisons:

Satish K. Aggarwal
Alan H. Cookson
Chester C. Taylor

Rochelle L. Stern
IEEE Standards Project Editor

Contents

IEEE Standard Test Specification for Thyristor Diode Surge Protective Devices

1. Overview

1.1 Scope

This standard applies to two or three terminal, four or five layer, thyristor surge protection devices (SPDs) for application on systems with voltages equal to or less than 1000 V rms or 1200 V dc. These protective devices are designed to limit voltage surges on communication circuits and on power circuits operating from direct current (dc) to 420 Hz. The thyristor SPD can be manufactured with unidirectional or bidirectional, symmetrical, or asymmetrical V-I characteristics. This standard contains definitions, service conditions, and a series of test criteria for determining the characteristics of a thyristor SPD. If the characteristics differ with the direction of conduction, each polarity shall be separately specified.

1.2 Tests

The tests in this standard are intended as design tests as defined in [B3][1] and provide a means of comparison among various thyristor SPDs.

NOTE—Three terminal devices may consist of multiple thyristor elements, or thyristor and diode elements, in one package; or the third may connect to the gate of a thyristor.

1.3 Applicability and device function

Thyristor SPDs are designed to conduct the surge currents necessary to provide overvoltage protection in electrical circuits. The purpose of this document is to provide definitions and test methods for thyristor SPD that are used for the protection of telecommunications systems. Overvoltage threats originate from lightning and ac power lines. These threats appear in the system through induction or direct contact. The waveforms that are used in the tests are chosen to allow confirmation of manufacturer's data.

[1]The numbers in brackets correspond to those publications listed in the bibliography, Annex B.

Other types of thyristors may exhibit similar characteristics. If they are used as thyristor SPDs, their surge suppression capabilities may be characterized according to this specification.

The thyristor SPDs exhibit a relatively high impedance in the off-state condition at normal system operating voltages before and after the surge. During the surge of sufficient voltage and current, the device will switch to a low-impedance (on-state) condition. After the surge has passed, the device is expected to recover to a high-impedance (off-state) condition. Consideration should be given to service conditions, temperatures, and device mounting when applying these parameters as variations may occur.

2. Definitions of rated and other parameters

2.1 Rated parameter values

For the purpose of this standard, the values of rated parameters are established by the manufacturer, according to statistical acceptance criteria as indicated in 4.2.

2.2 Definitions

The following apply specifically to thyristor SPDs and do not necessarily cover other devices. If the voltampere characteristics are asymmetrical, then the parameters shall be defined for each polarity.

The relation between some common terms on some typical device V-I graphs are illustrated in Figures 1–7. The characteristics of devices in the breakdown region can be complex and difficult to measure. All the points shown on the graphs may not be apparent on the actual device characteristic, and there may be additional inflection points not shown. Conceptually, all of the points will exist for every device, although points such as switching (V_s, I_s) and breakover $V_{(BO)}$, $I_{(BO)}$ may be nearly coincidental. Device specifications should only describe the relevant characteristics. For the method of defining impulse waveforms, see Figure 7 of [B2]. The minimum data that a manufacturer shall supply are those parameters listed in 2.2.1 through 2.2.13.

2.2.1 breakover current *($I_{(BO)}$)*: The instantaneous current flowing at the breakover voltage. (See 4.5.4 and Figures 1–7.)

2.2.2 breakover voltage *($V_{(BO)}$)*: The maximum voltage across the device in or at the breakdown region measured under specified voltage rate of rise and current rate of rise. (See 4.5.4 and Figures 1–7).

2.2.3 holding current *(I_H)*: The minimum current required to maintain the device in the on-state. (See 4.5.6 and Figures 1–7.)

2.2.4 non-repetitive peak on-state current *(I_{TSM})*: Rated maximum (peak) value of ac power frequency on-state surge current of specified wave shape and frequency which may be applied for a specified time or number of ac cycles. (See 4.4.3 and Figures 1–7.)

2.2.5 non-repetitive peak pulse current *(I_{PPS})*: Rated maximum value of peak impulse pulse current of specified amplitude and wave shape that may be applied. (See 4.4.4 and Figures 1–7.)

2.2.6 off-state capacitance *(C_O)*: The capacitance in the off-state measured at specified frequency, *f*, amplitude, V_d, and dc bias, V_D. (See 4.5.7.)

2.2.7 off-state current *(I_D)*: The dc value of current that results from the application of the off-state voltage. (See 4.5.1 and Figures 1–7.)

2.2.8 off-state voltage *(V_D)*: The dc voltage when the device is in the off-state. (See 4.5.1 and Figures 1–7.)

2.2.9 on-state current *(I_T)*: The current through the device in the on-state condition. (See 4.5.5 and Figures 1–7.)

2.2.10 on-state voltage *(V_T)*: The voltage across the device in the on-state condition at a specified current. (See 4.5.5 and Figures 1–7.)

2.2.11 repetitive peak off-state current *(I_{DRM})*: The maximum (peak) value of off-state current that results from the application of the repetitive peak off-state voltage. (See 4.5.2 and Figures 1–6.)

2.2.12 repetitive peak off-state voltage *(V_{DRM})*: Rated maximum (peak) continuous voltage that may be applied in the off-state conditions including all dc and repetitive alternating voltage components. (See 4.4.1 and Figures 1–6.)

2.2.13 repetitive peak on-state current *(I_{TRM})*: Rated maximum (peak) value of ac power frequency on-state current of specified wave shape and frequency which may be applied continuously. (See 4.4.2 and Figures 1–7.)

2.3 Additional definitions

For certain applications some of the following terms may be necessary or useful. Listed also are those parameters specific to certain thyristor SPD technologies.

2.3.1 breakdown current *($I_{(BR)}$)*: The current through the device in the breakdown region. (See 4.5.8 and Figures 1–3.)

2.3.2 breakdown voltage *($V_{(BR)}$)*: The voltage across the device in the breakdown region (prior to the switching point) at a specified breakdown current, $I_{(BR)}$. (See 4.5.8 and Figures 1–3.)

2.3.3 critical rate of rise of off-state voltage *(dv/dt)*: The maximum rate of rise of voltage (below V_{DRM}) that will not cause switching from the off-state to the on-state. (See 4.5.12.)

2.3.4 critical rate of rise of on-state current *(di/dt)*: Rated value of the rate of rise of current which the device can withstand without damage. (See 4.4.8.)

2.3.5 forward current *(I_F)*: The current through the device in the forward conducting state. (See 4.5.10 and Figures 3 and 6.)

2.3.6 forward voltage *(V_F)*: The voltage across the device in the forward conducting state at a specified current I_F. (See 4.5.10 and Figures 3 and 6.)

2.3.7 impulse reset time *($t_{(Reset)}$)*: The time taken for a device to switch back into the off-state, in the presence of a specified value of dc short-circuit current, after being switched into the on state by a specified impulse. (See 4.5.13.)

2.3.8 insulation resistance: The equivalent insulation resistance of the device, computed by

$$\frac{V_D}{I_D}$$ (See 4.5.1.)

2.3.9 lifetime rated pulse currents: Rated values of the peak impulse current, I_{PP}, as a function of the number of pulses and wave shape, which may be applied over the device rated lifetime. (See 4.4.3 and 4.4.4.)

2.3.10 non-repetitive peak forward current (I_{FSM}): Rated maximum (peak) value of ac power frequency forward surge current of specified wave shape and frequency which may be applied for a specified time or number of ac cycles. (See 4.4.6 and Figures 3 and 6.)

2.3.11 peak pulse impulse current (I_{PPM}): Rated maximum value of peak impulse pulse current (I_{PP}) applied for 10 pulses with 10 × 1000 μs waveform and maximum duty factor of 0.01% without causing failure. Refer to [B6]. (See 4.4.4.)

2.3.12 peak forward recovery voltage (V_{FRM}): The maximum value of forward conduction voltage across the device upon the application of a specified voltage rate of rise and current rate of rise following a zero or specified reverse-voltage condition. (See 4.5.11.)

2.3.13 repetitive peak forward current (I_{FRM}): Rated maximum (peak) value of ac power frequency forward current of specified wave shape and frequency which may be applied continuously. (See 4.4.7 and Figures 3 and 6.)

2.3.14 repetitive peak reverse current (I_{RRM}): The maximum (peak) value of reverse current that results from the application of the repetitive peak reverse voltage, V_{RRM}. (See 4.5.3 and Figures 1 and 4.)

2.3.15 repetitive peak reverse voltage (V_{RRM}): Rated maximum (peak) continuous voltage that may be applied in the reverse blocking direction including all dc and repetitive alternating voltage components. (See 4.4.5 and Figures 1 and 4.)

2.3.16 switching current (I_S): The instantaneous current flowing through the device at the switching voltage, V_S. (See 4.5.9 and Figures 1–7.)

2.3.17 switching resistance (R_s): The equivalent slope resistance of the breakdown region, R_S, computed by

$$\frac{(V_{(BO)} - V_S)}{(I_S - I_{(BO)})}$$

(See 4.5.9, 4.5.4, and Figures 4 –6.)

2.3.18 switching voltage (V_S): The instantaneous voltage across the device at the final point in the breakdown region prior to switching into the on-state. (See 4.5.9 and Figures 1–7.)

2.4 Temperature dependence of parameters

2.4.1 maximum junction temperature (T_{JM}): The maximum value of permissible junction temperature, due to self heating, which a thyristor SPD can withstand without degradation. (See 4.5.17–4.5.18.)

2.4.2 temperature coefficient of breakdown voltage ($\alpha_{V(BR)}$); ($dV_{(BR)}/dT_J$): The ratio of the change in breakdown voltage, $V_{(BR)}$, to changes in temperature. Expressed as either millivolts per degree Celsius (mV/°C), or percent per degree Celsius (%/°C) with reference to the 25 °C value of breakdown voltage (mV/°C or %/°C). (See 4.5.14.)

2.4.3 temperature derating: Derating with temperature above a specified base temperature, expressed as a percentage, such as may be applied to peak pulse current (See 4.5.16.)

2.4.4 thermal resistance ($R_{\theta JL}$; $R_{\theta JC}$; $R_{\vartheta JA}$) : The effective temperature rise per unit power dissipation of a designated junction, above the temperature of a stated external reference point (lead, case, or ambient) under conditions of thermal equilibrium. (See 4.5.17.)

2.4.5 transient thermal impedance ($Z_{\theta JL(t)}$; $Z_{\theta JC(t)}$; $Z_{\theta JA(t)}$) : The change in the difference between the virtual junction temperature and the temperature of a specified reference point or region (lead, case, or ambient) at the end of a time interval divided by the step function change in power dissipation at the beginning of the same time interval that causes the change of temperature-difference. (See 4.5.18.)

NOTE— It is the thermal impedance of the junction under conditions of change and is generally given in the form of a curve as a function of the duration of an applied pulse.

2.4.6 variation of holding current with temperature: The change in holding current, I_H, with changes in temperature. It is shown as a graph. (See 4.5.15.)

2.4.7 virtual junction temperature (T_J): A theoretical temperature representing the temperature of the junction(s) calculated on the basis of a simplified model of the thermal and electrical behavior of the device. (See 4.5.17–4.5.18.)

2.5 Gated thyristor surge protection device (SPD)

These devices have a gate (*G*, *g*) terminal that controls the switching region characteristics and the main terminals provide the SPD function. Two gate types are possible, as this additional terminal may be connected to either an intermediate p or n layer of the thyristor. The first is a p-gate device, which has the gate biased negatively with respect to the anode. The p-gate device provides negative transient voltage protection with respect to the anode. The second is an n-gate device, which has the gate biased positively with respect to the cathode. The n-gate device provides positive transient voltage protection with respect to the cathode.

The gated thyristor SPD has many forms. Options are single or dual switching quadrant, n-gate and/or p-gate, forward or reverse conducting or blocking quadrants. The following definitions give the terms and parameters in general form with specific devices detailed, including the symbol and references in parentheses.

2.5.1 gate reverse current, adjacent terminal open (I_{GAO}; I_{GKO}): The current through the gate terminal when a specified gate bias voltage, V_G, is applied and the cathode terminal for a p-gate device or anode terminal for an n-gate device is open circuited. (See 4.5.20, common-gate configuration.)

2.5.2 gate reverse current, main terminals short-circuited (I_{GAS}; I_{GKS}): The current through the gate terminal when a specified gate bias voltage, V_G, is applied and the cathode terminal for a p-gate device or anode terminal for an n-gate device is short circuited to the third terminal. (See 4.5.2.)

2.5.3 gate reverse current, on-state (I_{GAT}; I_{GKT}): The current through the gate terminal when a specified gate bias voltage, V_G, is applied and a specified on-state current, I_T, is flowing. (See 4.5.22 and Figure 7b).

2.5.4 gate reverse current, forward conducting state *(I_{GAF}; I_{GKF})*: The current through the gate terminal when a specified gate bias voltage, V_G, is applied and a specified forward conduction current, I_F, is flowing. (See 4.5.23.)

2.5.5 gate switching charge *(Q_{GS})*: The charge through the gate terminal, under impulse conditions, during the transition from the off-state to the switching point, when a specified gate bias voltage, V_G, is applied. (See 4.5.24.)

2.5.6 gate-to-adjacent terminal breakover voltage *($V_{GK(BO)}$; $V_{GA(BO)}$)*: The gate to cathode voltage for a p-type device or gate to anode voltage for an n-gate device at the breakover point. This is equivalent to the voltage difference between the breakover voltage, $V_{(BO)}$, and the specified gate voltage, V_G. (See 4.5.26.)

2.5.7 gate-to-adjacent terminal peak off-state voltage *(V_{GDM})*: The maximum gate to cathode voltage for a p-gate device or gate to anode voltage for an n-gate device that may be applied such that a specified off-state current, I_D, at a rated off-state voltage, V_D, is not exceeded. (See 4.5.19.)

2.5.8 peak off-state gate current *(I_{GDM})*: The maximum gate current that results from the application of the peak off-state gate voltage, V_{GDM} . (See 4.5.19.)

2.5.9 peak gate switching current *(I_{GSM})*: The maximum value of current through the gate terminal during the transition from the off-state to the switching point, when a specified gate bias voltage, V_G, is applied. (See 4.5.25 and Figure 7b).

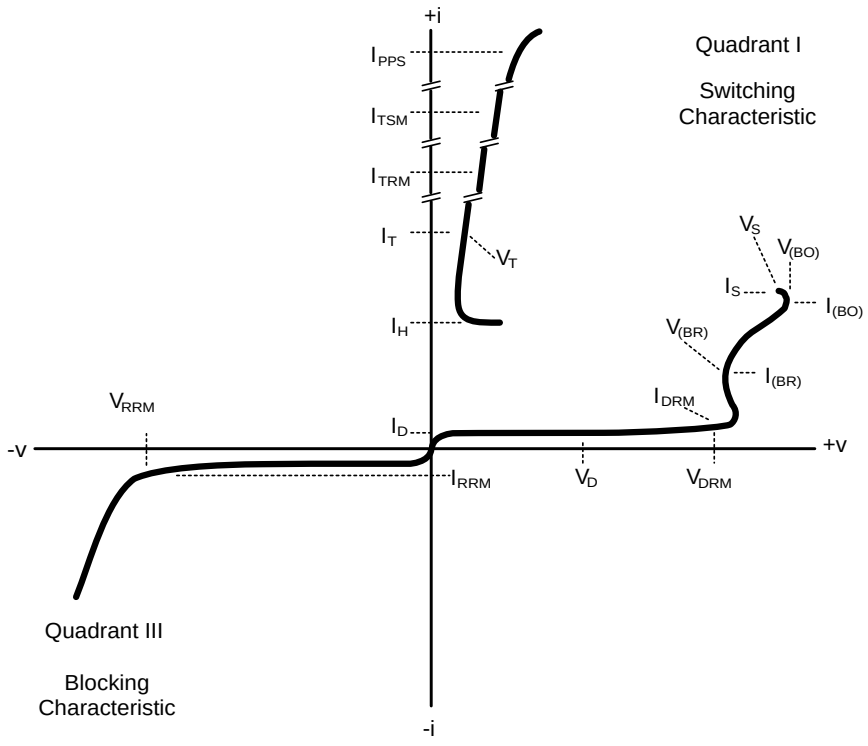


Figure 1—Graph illustrating symbols of terms for a reverse blocking positive breakdown slope thyristor SPD

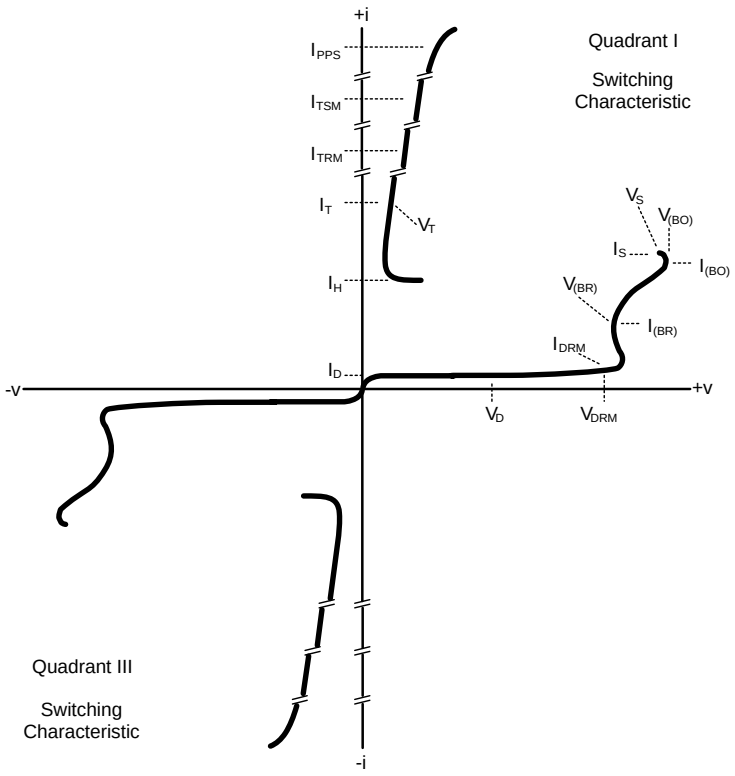


Figure 2—Graph illustrating symbols of terms for a bidirectional positive breakdown slope thyristor SPD

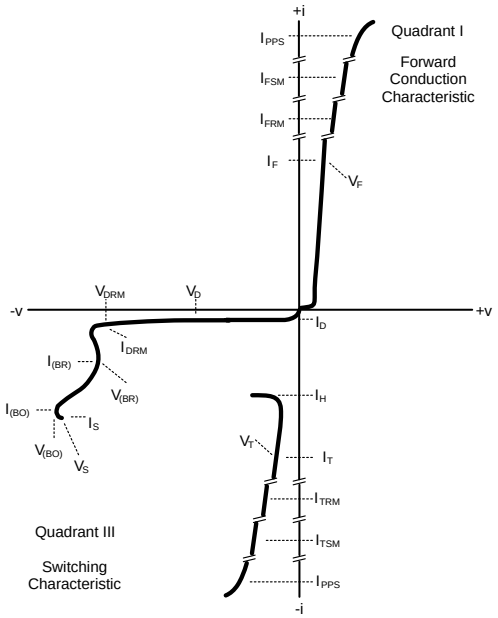


Figure 3—Graph illustrating symbols of terms for a forward conducting positive breakdown slope thyristor SPD

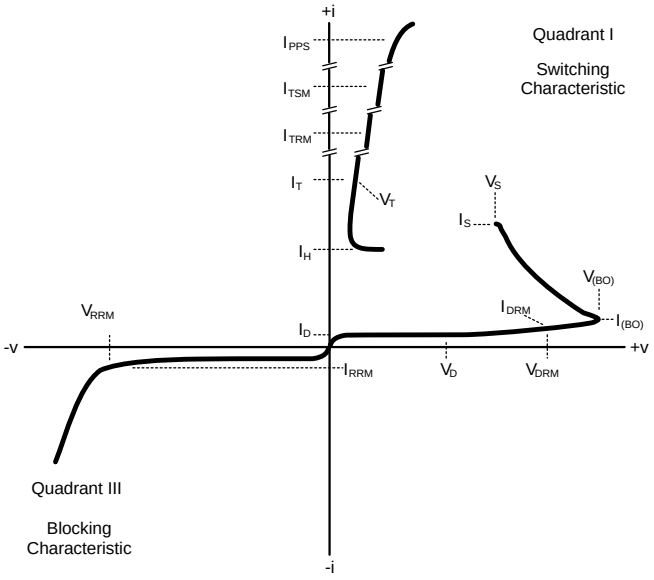


Figure 4—Graph illustrating symbols of terms for a reverse blocking negative breakdown slope thyristor SPD

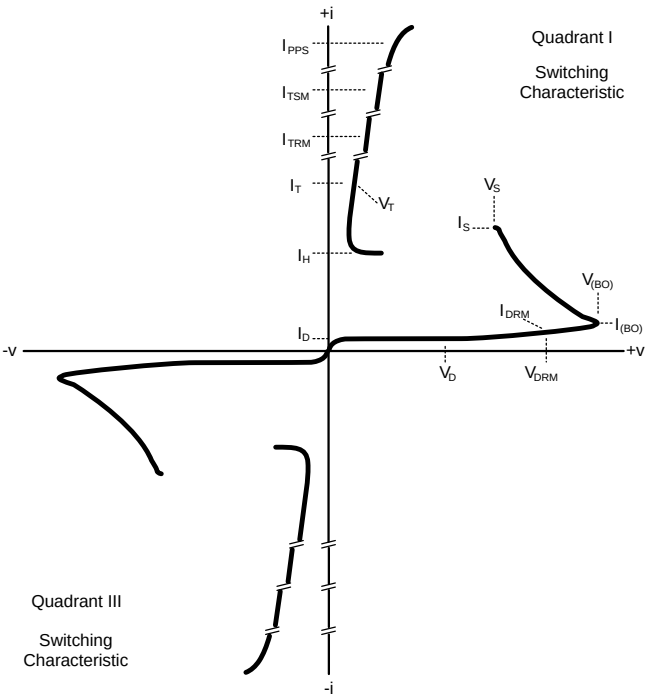


Figure 5—Graph illustrating symbols of terms for a bidirectional negative breakdown slope thyristor SPD

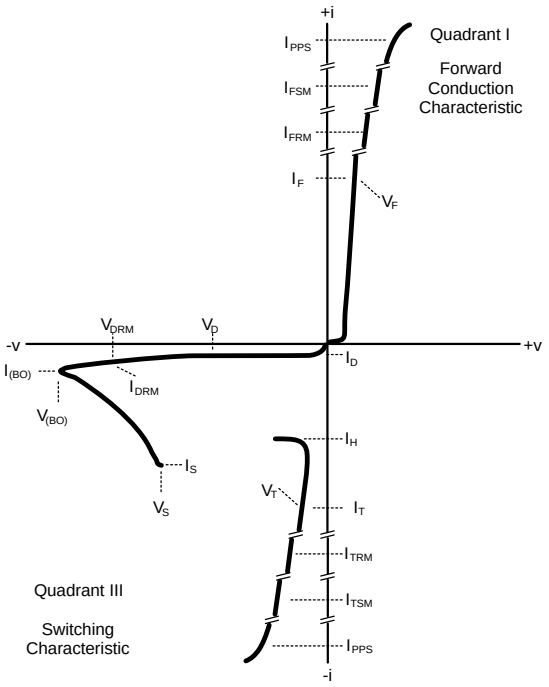


Figure 6—Graph illustrating symbols of terms for a forward conducting negative breakdown slope thyristor SPD

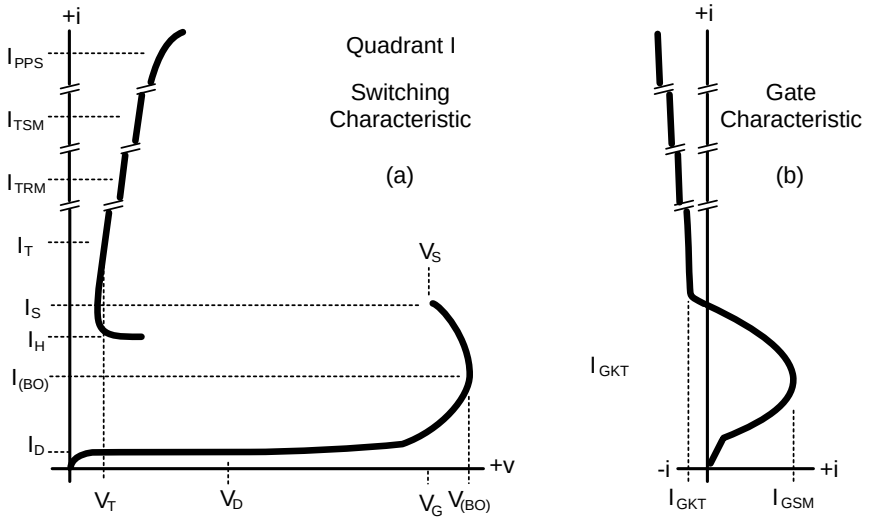


Figure 7—Graph illustrating symbols of terms for a gated thyristor SPD

3. Service condition

3.1 Normal service conditions

Thyristor SPDs conforming to this standard shall be rated for climatic ranges of temperature, humidity, and pressure. In the absence of special requirements, it is recommended that the listed values should be used. Some service conditions relate to the mandatory parameters of 2.2. This relationship is shown in parenthesis. Any other service condition should be specified by the manufacturer or requested by the user, as appropriate.

3.1.1 Climatic conditions

a) Operating temperature range
   1) normal: 0 °C to 70 °C
   2) extended: –40 °C to 85 °C
b) Storage temperature range
   1) normal: –40 °C to 150 °C
   2) extended: –65 °C to 150 °C
c) Humidity range
   1) normal: 20% to 75%
   2) extended: 10% to 100%
d) Air pressure range
   1) normal: 86 kPa to 106 kPa
   2) extended: 70 kPa to 106 kPa

3.1.2 Other environmental conditions

a) Mechanical shock
b) Mechanical vibration

3.1.3 Physical properties

a) Solvent resistance
b) Solderability
c) Flammability
d) Package rupture during overload
e) Electrical connection to metal case

3.1.4 System conditions

a) Nominal systems frequencies (off-state capacitance)
b) Maximum continuous system voltage and current (repetitive peak off-state voltage, off-state current and holding current)
c) Peak impulse currents (non-repetitive peak pulse current)
d) Peak power frequency ac currents (non-repetitive peak on-state current)
e) Surge repetition rate

3.1.5 Surge rating of the thyristor SPD under system conditions

a) Rated non-repetitive peak current
b) Rated non-repetitive peak pulse current temperature derating
c) Lifetime rated pulse currents

3.2 Unusual service conditions

The following service conditions may require special consideration in the design or application of thyristor diodes and should be called to the attention of the manufacturer.

3.2.1 Environmental conditions

a) Climatic conditions
   1) Temperature, humidity and pressure values exceeding normal service conditions
   2) Precipitation (rain, snow and hail)
   3) Other water sources (dipping, splashing, steam, submersion, condensation, ice, and frost formation)
b) Biological conditions
   1) Flora
   2) Fauna
c) Chemically active substances
   1) Damaging fumes or vapors
   2) Salt spray
   3) Flammable or explosive atmosphere
d) Mechanically or electrically active substances
   1) Dust
   2) Soot
e) Contaminating fluids
f) Mechanical conditions
   1) Vibration (stationary or shock)
   2) Drop (stationary or shock)
g) Impact
h) Static load
i) ESD

3.2.2 Physical conditions

Limitation on weight or dimension, including clearance to nearby conducting objects.

3.2.3 System conditions

a) Electrical system conditions. Sustained overvoltages, temporary overvoltage (TOV), current conductive rates, or frequency operating conditions whereby the ratings of the devices are exceeded (see Clause 5, Failure modes).
b) System impulse currents not within the rating of the device (see Clause 5, Failure modes).
c) Exposure to direct lightning strike (see Clause 5, Failure modes).
d) Electromagnetic field effects (see Clause 5, Failure modes).
e) Unusual ground potential situations (see Clause 5, Failure modes).
f) Any other unusual condition known to the user.

4. Standard design test procedure

4.1 Standard design test criteria

The design test described in 4.4.1 through 4.5.26 provide standardized methods for making single observations of a specified property of a thyristor SPD. These properties may vary from device to device making it necessary to provide statistical descriptions of the property in order to compare products.

4.2 Statistical analysis

The following procedure shall be used to describe any characteristics that have been determined to have important statistical aspects. A product sample shall be chosen in a manner consistent with the definition of design tests as provided by [B3]. A sufficient number of devices shall be tested and the characteristics in question measured or ratings verified as described in the applicable design test until the parameters of the underlying statistical distribution are determined within confidence limits specified by the manufacturer. Values relating to the product sample such as, but not limited to, mean, maximum, and standard deviation may then be stated.

Certain device parameters, particularly current ratings, will be dependent on several equally dominant mechanisms, and the resulting parameter distribution will be multi-modal. Applying normal distribution statistics to multi-modal distributions can give serious errors in the prediction of distribution tail limits. In these cases, alternative statistical procedures should be used to enable accurate prediction of the distribution tails (e.g., Weibull plots).

4.3 Thyristor surge protection device (SPD) test conditions

The tests of 4.4.1 through 4.5.26 should be performed on the thyristor SPD either as required by the application or as detailed in the device specification. The thyristor SPD shall be tested with the specified environmental conditions, such as temperature range, and mounting configuration. Unless otherwise specified, the reference ambient test conditions should be as follows:

a) Temperature: 25 ±5 °C;
b) Relative humidity: less than 85%.

Measurement errors can be caused by ground loops, common impedances, magnetic induction, electric induction, and electromagnetic radiation. The voltage error caused by a circulating ground-loop current can be reduced by increasing the loop impedance. Normally this would be done by clipping ferrite cores on to the probe cables. Common impedances can be avoided by using kelvin contacts to the device under test (DUT) for power and sense connections. Magnetic induction and inductive effects can be reduced by short lead lengths and minimizing the wiring loop area, possibly by using twisted wires. Electric induction (capacitive pickup) can be removed by interposing a Faraday shield connected to a non-signal ground. Electromagnetic pickup can be reduced by shielding and the techniques used for magnetic induction.

Analog oscilloscopes should have rise times five times faster than the signal rise time. This will ensure less than a 2% error in the displayed rise time. Digital oscilloscopes should have sample times at least five and preferably 20 times faster than the signal rise time. Eight-bit digital oscilloscopes may not have sufficient measurement resolution, unless enhanced by sample averaging or use of a calibrated offset voltage to window the signal. Ten bit digital oscilloscopes will usually have sufficient resolution without the aid of these techniques.

Because of the voltage and energy levels used in most of the tests, all tests should be considered hazardous. Appropriate caution should be taken in their performance. Non-electrical hazards may be produced, such as fire, heat, fragmentation, and fumes.

4.3.1 Wave shape and values

The wave shape of an impulse is designated by a combination of two numbers. The first, an index of the wavefront, is the virtual duration of the wavefront in microseconds. The second, an index of the wave tail, is the time in microseconds from the virtual zero to the instant at which one-half the crest (peak) value is reached on the wave tail (see [B4]).

The quoted thyristor SPD current ratings are the short-circuit test generator values. Under test conditions the actual device current will be different, due to the interaction of the generator with the device characteristic.

4.3.2 Multiple thyristor SPDs

Where multiple thyristor SPDs are packaged together and the application simultaneously operates them, if the individual SPD parameters are significantly affected by the operation of the other SPDs, the testing shall emulate this condition as well as single SPD operation.

4.3.3 Gated thyristor SPD test conditions

All fixed voltage thyristor SPD tests shall be performed on a gated thyristor SPD to verify and determine the protection terminal performance. Gated thyristor SPDs shall be tested with the appropriate values of gate bias voltage, V_{GG}, and network. Unless otherwise specified, the gate bias voltages used for testing shall be the maximum and minimum values of the intended application. For any tests where the gated thyristor SPD limits the voltage, the gate supply should be low impedance (decoupled) and a thyristor SPD without internal gate blocking shall have an appropriately poled blocking diode connected directly in series with the gate terminal. When a gated thyristor SPD has been designed to give gate controlled and fixed voltage protection, the fixed voltage thyristor SPD tests shall also be performed with the gate open circuit (i.e., $I_G = 0$).

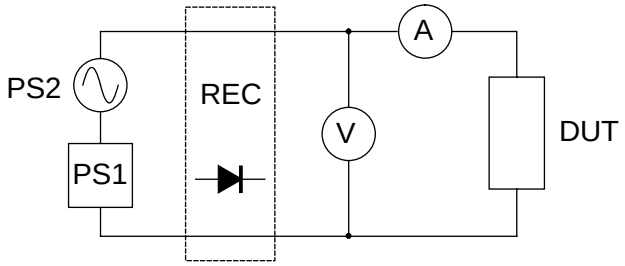
4.4 Rating test procedures

4.4.1 Repetitive peak off-state voltage— V_{DRM}

The purpose of this test is to verify that the thyristor SPD maintains a high-impedance off-state condition when continuously subjected to the rated repetitive peak off-state voltage. The rated value of repetitive peak off-state voltage, V_{DRM}, shall be impressed across the device and the value of repetitive peak off-state current, I_{DRM}, measured during the test conducted with a circuit functionally equivalent to Figure 8. The measured current shall not exceed the maximum specified value of I_{DRM}. After the V_{DRM} test, the device shall not fail any of its specified characteristics. The test duration shall be long enough to establish the desired confidence in device reliability. Each switching quadrant of the thyristor SPD shall be separately tested and measured. (Large changes between pre- and post-test characteristics are a possible indication of device degradation.) Test failures shall be classified according to the criteria of Clause 5.

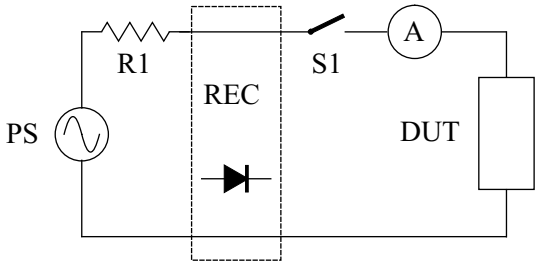
4.4.2 Repetitive peak on-state current— I_{TRM}

The purpose of this test is to verify that the thyristor SPD can continuously conduct its rated repetitive peak (quasi-sinusoidal) on-state current without failure or exceeding the maximum rated junction temperature (see Figure 10). The test circuit used shall be functionally equivalent to Figure 9. The ac test generator shall be specified for the open-circuit voltage and short-circuit current values, or equivalents, of wave shape and wave shape peak value. The capability of the generator shall ensure that the thyristor SPD will always switch into the on-state. Unidirectional thyristor SPDs, which are not rated for bidirectional current operation, will require a bridge or half-wave rectifier to be added to the ac voltage source for full or half wave testing. During the I_{TRM} test, a temperature sensitive device parameter, such as I_H, can be monitored by means of an oscilloscope whose current and voltage probes are connected to the DUT in the manner shown in Figure 13. The average working junction temperature can be calculated from the measured parameter values, the parameter temperature coefficient and the DUT initial temperature. After the I_{TRM} test, the device shall not fail any of its specified characteristics. The test duration shall be long enough to establish the desired confidence in device reliability. (Large changes between pre- and post-test characteristics are a possible indication of device degradation.) Test failures shall be classified according to the criteria of Clause 5.



DUT = Device under test
A = Ammeter, peak reading
V = Voltmeter, mean, peak and ac reading
PS1 = DC power supply set to the dc component of V_{DRM}
PS2 = AC power supply set to the ac component of V_{DRM}
REC = Full or half-wave rectifier circuit, used for unidirectional testing when the ac component of V_{DRM} reverses the polarity

Figure 8—Test circuit for verifying repetitive peak off-state voltage (V_{DRM})



DUT = Device under test
A = Ammeter, peak reading current monitor
PS = AC power supply, set at specified voltage
R1 = Resistor, defines peak short circuit current
S1 = Switch, close to perform test
REC = Full or half-wave rectifier circuit, connected for unidirectional testing

Figure 9—Test circuit for verifying repetitive peak on-state current (I_{TRM})

4.4.3 Non-repetitive peak on-state current— I_{TSM}

The purpose of this test is to verify that the thyristor SPD can survive a specified duration of (quasi-sinusoidal) ac surge current without failure. The test circuit used shall be functionally equivalent to Figure 11. Switch S1 only opens or closes at the zero voltage crossings of the ac voltage source. This ensures that the device will be tested with complete half or full ac cycles. The ac test generator shall be specified for the open-circuit voltage and short-circuit current values, or equivalents, of wave shape, wave shape peak value, and duration for which switch S1 closes. The capability of the generator shall ensure that the thyristor SPD will always switch into the on-state. Unidirectional thyristor SPDs, which are not rated for bidirectional current operation, will require a bridge or half-wave rectifier to be added to the ac voltage source for full or half wave testing. After switch S1 has operated for the specified test duration and the device has returned to

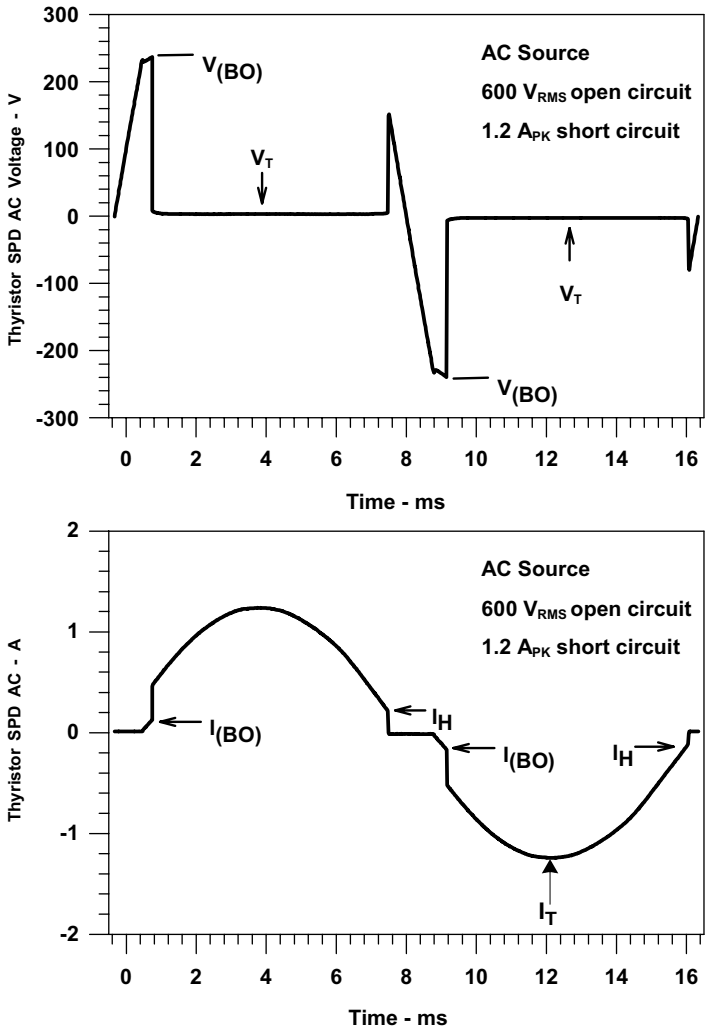


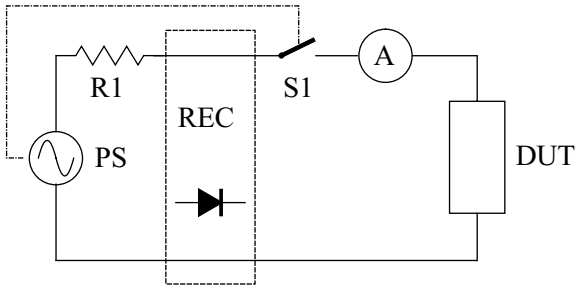
Figure 10—Repetitive peak on-state current waveforms

thermal equilibrium conditions, the device shall not fail any of its specified characteristics. (Large changes between pre- and post-test characteristics are a possible indication of device degradation.) Test failures shall be classified according to the criteria of Clause 5.

The test duration may be specified as a time or number of ac cycles at a specified power frequency. A non-repetitive current rating test shall not be repeated until the device has returned to thermal equilibrium conditions. In the absence of special requirements, it is recommended that the device shall be capable of withstanding up to 100 such tests without failure during its lifetime. The I_{TSM} rating will vary with test duration time and several values may be needed to fulfill an application need; recommended time durations are one cycle, 0.1 s, 1 s, and 10 s.

4.4.4 Non-repetitive peak pulse current— I_{PPS}

The purpose of this test is to verify that a thyristor SPD can survive a specified impulse wave shape of short-circuit current amplitude I_{PPS} without failure. The test circuit used shall be functionally equivalent to Figure 12. The impulse test generator shall be specified for the open-circuit voltage and short-circuit current values, or equivalents, of wave shape and wave shape peak value. The capability of the generator shall ensure that the thyristor SPD will always switch into the on-state. After the impulse and the device has



DUT = Device under test
A = Ammeter, peak reading current monitor
PS = AC power supply, set at specified voltage
R1 = Resistor, defines peak short circuit current
S1 = Switch, closes for specified duration, operation synchronised to ac voltage zero crossings
REC = Full or half-wave rectifier circuit, connected for unidirectional testing

Figure 11—Test circuit for verifying non-repetitive peak on-state current (I_{TSM})

returned to thermal equilibrium conditions, the device shall not fail any of its specified characteristics. (Large changes between pre and post test characteristics are a possible indication of device degradation.) Test failures shall be classified according to the criteria of Clause 5.

Each switching quadrant of the thyristor SPD shall be separately tested and measured. A non-repetitive current rating test shall not be repeated until the device has returned to thermal equilibrium conditions. In the absence of special requirements, it is recommended that the device shall be capable of withstanding up to 100 such tests without failure during its lifetime. For the purpose of verification a smaller number of tests may be preferred. The I_{PPS} rating will vary with wave shape and several wave shape values may be needed to fulfill an application need. Table 1 shows some wave shapes commonly used to test thyristor SPDs for telecommunication applications.

4.4.5 Repetitive peak reverse voltage—V_{RRM}

The purpose of this test is to verify that the thyristor SPD maintains a high-impedance blocking state condition when continuously subjected to the rated repetitive peak reverse voltage. The rated value of repetitive peak reverse voltage, V_{RRM}, shall be impressed across the device in its blocking direction and the value of repetitive peak reverse current, I_{RRM}, measured during the test using a circuit functionally equivalent to Figure 8. The measured current shall not exceed the maximum specified value of I_{RRM}. After the V_{RRM} test the device shall not fail any of its specified characteristics. The test duration shall be long enough to establish the desired confidence in device reliability. (Large changes between pre- and post-test characteristics are a possible indication of device degradation.) Test failures shall be classified according to the criteria of Clause 5.

4.4.6 Non-repetitive peak forward current— I_{FSM}

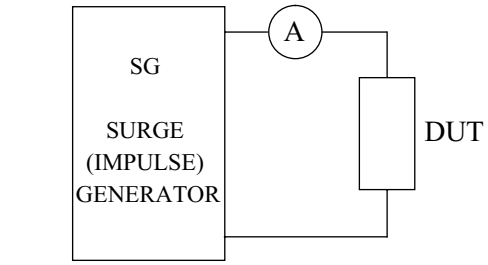
The purpose of this test is to verify that the diode section of a forward or reverse conducting thyristor SPD can survive a specified duration of ac surge current without failure. The test method for non-repetitive peak on-state current, I_{TSM} (see 4.4.3 and Figure 11), shall be used for verifying the non-repetitive peak forward current, I_{FSM}. If the conduction period used is one full cycle or longer, then I_{TSM} (see 4.4.3) rather than I_{FSM},

Table 1—Wave shapes used to test SPDs

Open-circuit voltage wave shape	Short-circuit current wave shape
2/10	2/10
1.2/50	8/20
10/160	10/160
10/560	10/560
10/700	5/310
10/1000	10/1000

NOTE— For the 1.2/50 generator, [B1] specifies the use of an external series resistance of 40 Ω minimum, when testing telecommunication lines. The available short-circuit current wave shape will then not be 8/20, but more like the 1.2/50 voltage wave shape.

is applicable. (I_{TSM} includes both diode and thyristor conduction.) After the I_{FSM} test and the device have returned to thermal equilibrium conditions, the device shall not fail any of its specified characteristics. (Large changes between pre- and post-test characteristics are a possible indication of device degradation.) Test failures shall be classified according to the criteria of Clause 5.



DUT = Device under test
A = Peak reading current monitor
SG = Impulse generator with specified characteristics

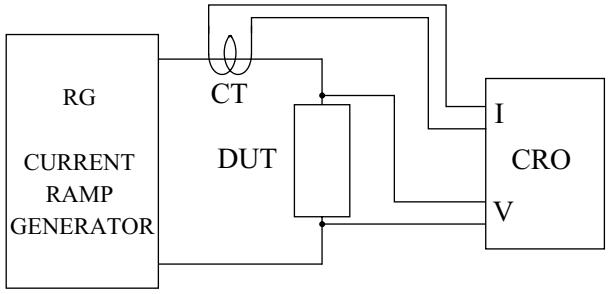
Figure 12—Test circuit for verifying non-repetitive peak pulse current (I_{PPS})

4.4.7 Repetitive peak forward current— I_{FRM}

The purpose of this test is to verify that the diode section of a forward or reverse conducting thyristor SPD can continuously conduct the rated repetitive peak forward current without failure or exceeding the maximum rated junction temperature. The test method for repetitive peak on-state current, I_{TRM} (see 4.4.2 and Figure 9), shall be used for verifying the repetitive peak forward current, I_{FRM}. In the absence of special requirements, it is recommended that I_{TRM} shall be specified instead of I_{FRM}, where I_{TRM} includes both diode and thyristor conduction.

4.4.8 Critical rate of rise of on-state current— *di/dt*

The purpose of this test is to verify that a thyristor SPD device can survive a fast rising current, as may occur on the wavefront of an impulse. The test circuit used shall be functionally equivalent to Figure 13. Voltage, *V*, and current, *I*, monitors (typically a digital or storage oscilloscope with voltage and current probes) are used to record the circuit conditions. After applying the *di/dt* impulse to the device, and when it has returned to thermal equilibrium conditions, the device shall not fail any of its specified characteristics. (Large changes between pre- and post-test characteristics are a possible indication of device degradation.) Test failures shall be classified according to the criteria of Clause 5.



DUT = Device under test
CT = Current transformer or equivalent
RG = Ramp generator with specified di/dt
CRO = Dual Channel Oscilloscope or equivalent

Figure 13—Test circuit for verifying critical rate of rise of on-state current (*di/dt*)

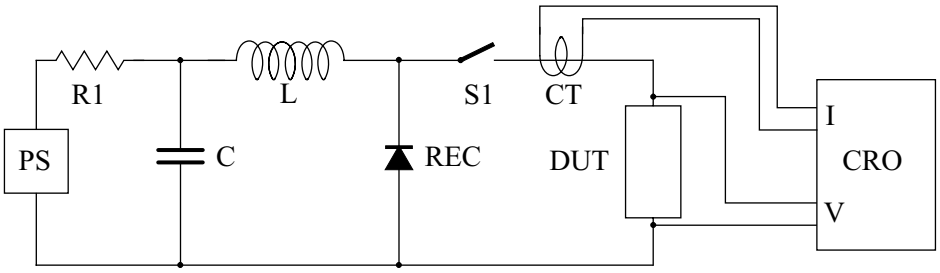
The *di/dt* test generator shall be specified for wavefront *di/dt* and peak (crest) current and wave shape (normally the wave tail will be relatively short). It is essential that the correct waveform is used for this test, and the device manufacturer should be contacted for the test circuit and waveform details. In the absence of special requirements, it is recommended that a generator based on the standard thyristor *di/dt* test circuit be used. The basic circuit diagram and its waveforms are shown in Figure 14.

Each switching quadrant of the thyristor SPD shall be separately tested and measured. A non-repetitive current rating test shall not be repeated until the device has returned to thermal equilibrium conditions. In the absence of special requirements, it is recommended that the device shall be capable of withstanding up to 100 such tests, in each test polarity, without failure, during its lifetime. For the purpose of verification a smaller number of tests may be preferred.

4.5 Characteristic test procedures

4.5.1 Off-state current— I_D

The purpose of this test is to determine the off-state current of a thyristor SPD when biased at a specified dc off-state voltage. The test circuit used shall be functionally equivalent to Figure 15. The voltage output of the dc supply shall be ramped from zero to the specified value of dc off-state voltage, V_D, at a rate below the minimum value of the critical rate of rise of off-state voltage. The dc voltage is applied until the value of off-state current, I_D, stabilizes. The final value of I_D shall be measured. Unless specified otherwise, each switching quadrant of the thyristor SPD shall be separately tested and measured.



DUT = Device under test
CT = Current transformer or equivalent
PS = DC power supply, set to V_S
R1 = Resistor, limits charging current
S1 = Switch, closes to start test; opens at current zero crossing
REC = Rectifier circuit, conducts negative current
C = Capacitor, energy storage and timing
L = Inductor, sets di/dt
CRO = Dual Channel Oscilloscope or equivalent

$V_S \gg V_{(BO)}$
$di/dt \approx V_S/L$
$I_{pk} \approx V_S(C/L)^{0.5}$
$t_W \approx \pi(LC)^{0.5}$

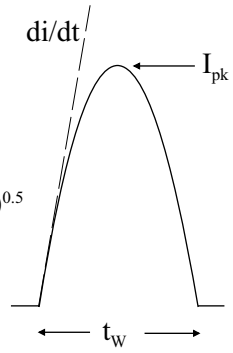
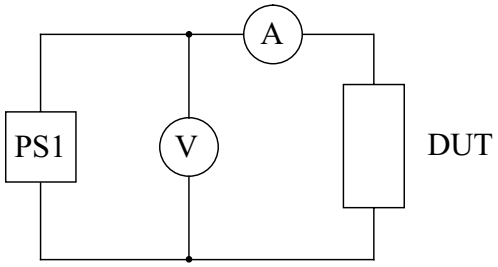


Figure 14—Half sine wave *di/dt* test circuit



DUT = Device under test
A = Microammeter
V = DC voltmeter
PS1 = DC power supply ramped to V_D

Figure 15—Test circuit for off-state current (I_D at V_D)

4.5.2 Repetitive peak off-state current— I_{DRM}

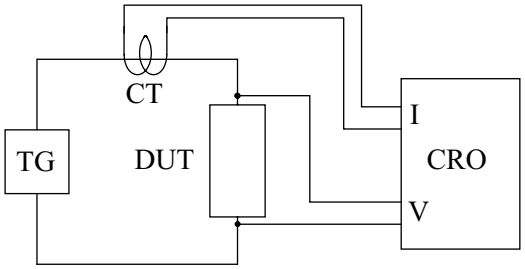
The purpose of this test is to determine the peak off-state current of a thyristor SPD when biased at the specified repetitive peak off-state voltage. The rated value of the repetitive peak off-state voltage, V_{DRM}, shall be impressed across the device and the value of device repetitive peak off-state current, I_{DRM}, measured during the test using a circuit functionally equivalent to Figure 8. Unless specified otherwise, each switching quadrant of the thyristor SPD shall be separately tested and measured.

4.5.3 Repetitive peak reverse current—I_{RRM}

The purpose of this test is to determine the peak reverse current of a reverse blocking thyristor SPD when biased at the specified repetitive peak reverse voltage. The rated value of repetitive peak reverse voltage, V_{RRM}, shall be impressed across the device in its blocking quadrant and the peak value of device repetitive peak reverse current, I_{RRM}, measured during a test using a circuit functionally equivalent to Figure 8.

4.5.4 Breakover voltage— $V_{(BO)}$ and current— $I_{(BO)}$

The purpose of this test is to determine the breakover of a thyristor SPD at a specified ramp rate. The test circuit used shall be functionally equivalent to Figure 16. The test generator shall be specified for the open-circuit voltage and short-circuit current values, or equivalents, of rate-of-rise, wave shape; wave shape peak value; and, for ac testing duration. Alternatively, the test generator circuit diagram shall be given. The peak voltage, $V_{(BO)}$, that occurs across the DUT in switching from the off-state to the on-state shall be measured (see Figures 17–19). For multiple cycle ac testing, the measured value shall be the highest value of all individual cycle $V_{(BO)}$ values. The corresponding instantaneous device current, $I_{(BO)}$, at $V_{(BO)}$ shall also be measured for a power frequency voltage ramp rate (see Figures 17–19).



DUT = Device under test
CT = DC current probe or equivalent
TG = Test generator with specified characteristics
switching DUT from off state to on state
CRO = Dual Channel Oscilloscope or equivalent

Figure 16—Test circuit for breakover ($V_{(BO)}$ and $I_{(BO)}$) and on-state voltage (V_T)

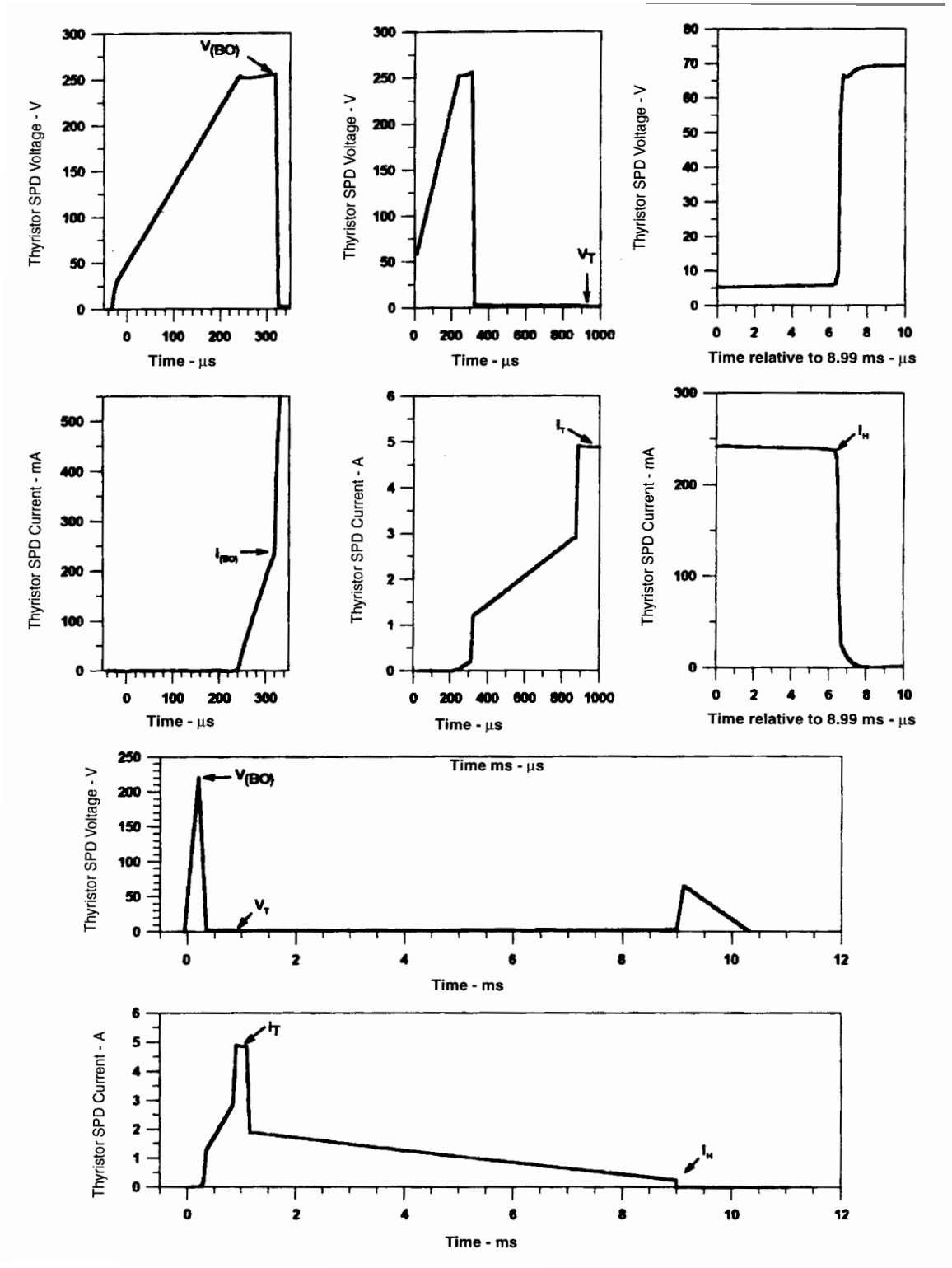


Figure 17—Switching and on-state waveforms for a positive breakdown slope thyristor SPD

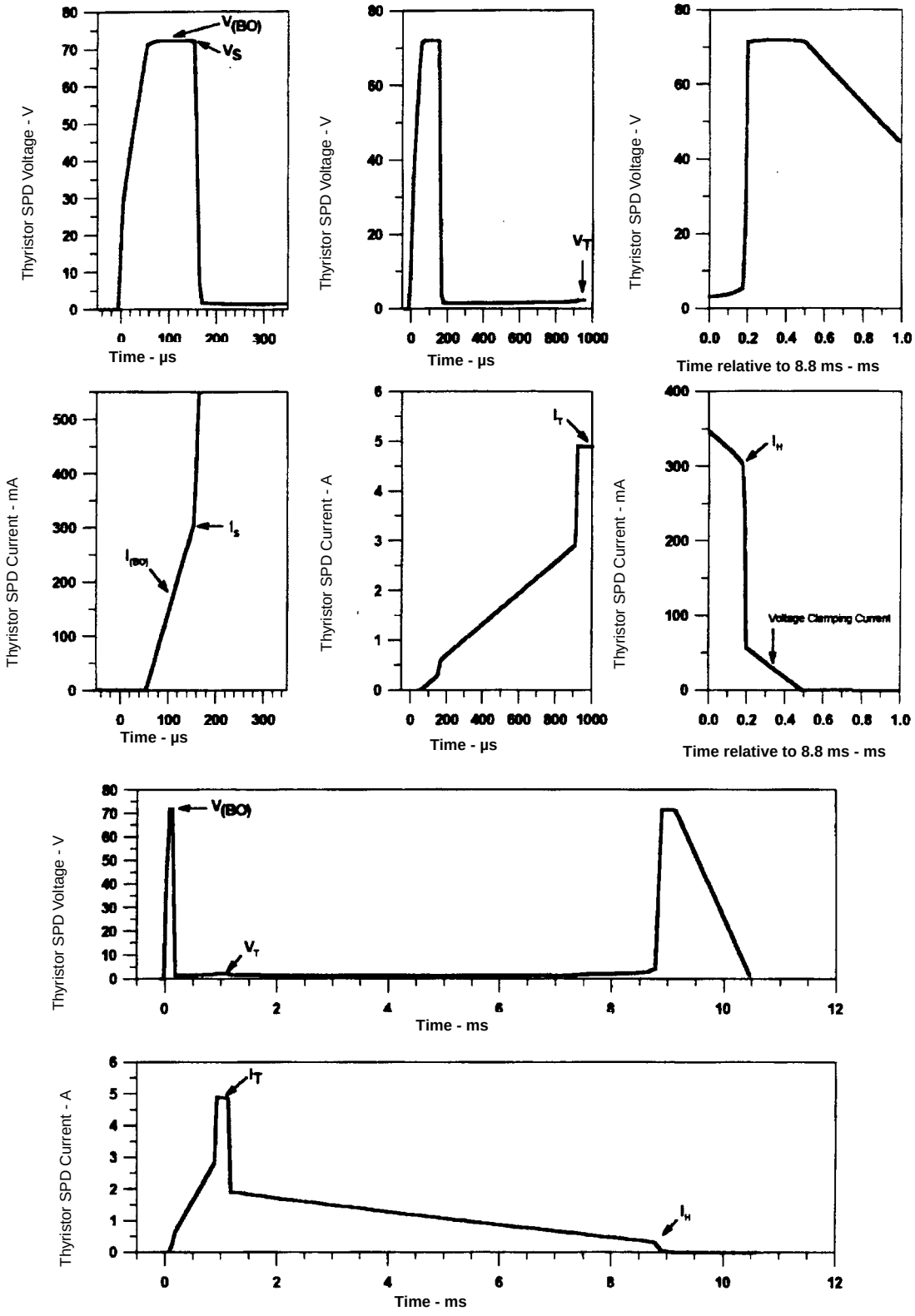


Figure 18—Switching and on-state waveforms of a gated thyristor SPD

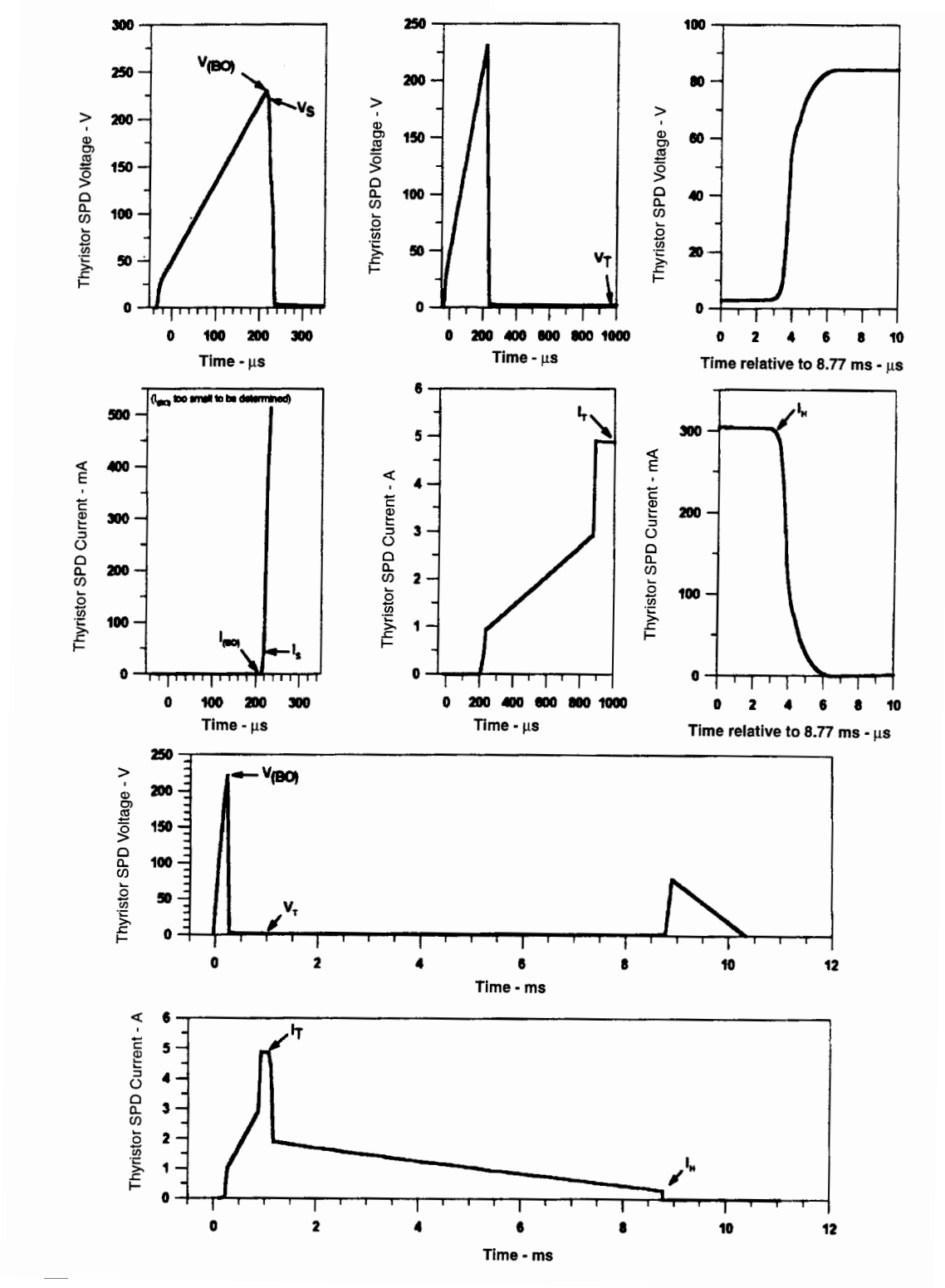


Figure 19—Switching and on-state waveforms for a negative breakdown slope thyristor SPD

Figures 17–19 show the switching quadrant voltage and current waveforms of the three thyristor SPD types—positive breakdown slope, negative breakdown slope, and gated. The bottom two waveforms separately show the overall thyristor SPD voltage and current. The top two rows of waveforms show expanded sections of the overall waveform to detail the clamping, on-state, and switch-off conditions. (Figures 1–7 showed the three device types in terms of the principal voltage-current characteristic.) The test generator consisted of a current source and a shunt 300 W resistor. Starting from zero the current source ramped to 3 A at 3.33 A/ms (1000 V/ms open-circuit voltage); the current then stepped to 5 A for 200 µs before dropping down to 2 A, after which the current ramped to zero at a rate of 0.2 A/ms. This sequence test exercises the device around its characteristic, enabling measurement of $V_{(BO)}$, $I_{(BO)}$, V_S, I_S, V_T, and I_H values, as appropriate, for the device. The waveforms shown illustrate the device type generic wave shapes and these should not be taken as typical values.

Each switching quadrant of the thyristor SPD shall be separately tested and measured. Multiple cycle ac testing of unidirectional thyristor SPDs shall be done with either full-wave or half-wave rectified ac as required by the application. The $V_{(BO)}$ and $I_{(BO)}$ values will vary with rate-of-rise and several ramp rates may be needed to fulfill an application need. In the absence of special requirements, it is recommended that the rates of rise shown in Table 2 be used for testing.

Table 2—Recommended breakover test ramps

Application	dv/dt	di/dt
ac	250 V/ms	1 A/ms
slow-wavefront impulse	100 V/µs	1 A/µs
fast-wavefront impulse	1000 V/µs	10 A/µs

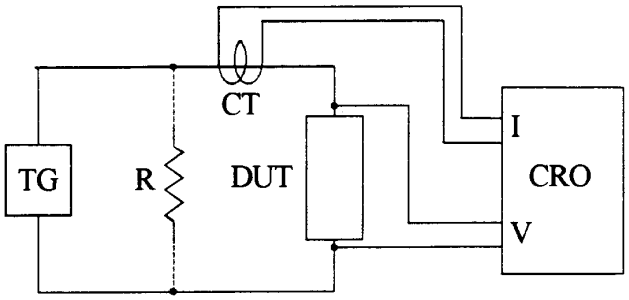
4.5.5 On-state voltage— V_T

The purpose of this test is to determine the on-state voltage of a thyristor SPD at a specified current; this voltage value is used to calculate the on-state power loss. The test circuit used shall be functionally equivalent to Figure 16. The test generator shall be specified for the open-circuit voltage and short-circuit current values, or equivalents, of wave shape and wave shape peak value. Alternatively, the test generator circuit diagram shall be given. The generator shall switch the DUT into the on-state condition, and the value of on-state voltage, V_T, shall be measured at a specified time or value of on-state current, I_T. (See V_T waveforms in Figures 17–19 and 4.5.4.) In the absence of special requirements, it is recommended that a time of 200 µs and a rectangular current impulse of 5 A be used for testing.

Each switching polarity of the thyristor SPD shall be separately tested and measured. The value of V_T will vary with the value of I_T and time. A low- and high-current value of V_T may be required to cover ac and impulse operation.

4.5.6 Holding current— I_H

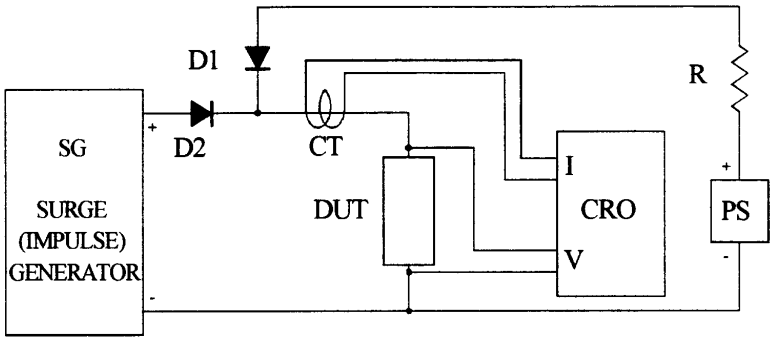
The purpose of this test is to determine the holding current of a thyristor SPD. The test circuit used shall be functionally equivalent to Figure 20. The test generator shall be specified for the open circuit voltage and short-circuit current values, or equivalents, of wave shape, and wave shape peak value. The generator shall switch the DUT into a specified on-state condition and then ramp down the on-state current until the device switches off (see I_H waveforms of Figures 17 to 19, and 4.5.4). Switch off is determined when the device voltage value exceeds a specified threshold level. The instantaneous value of the extrapolated ramp of when this occurs is measured as the holding current. This established approach measures the current at which the device is switching off, rather than the current at which the device is just maintaining its on state. In most applications, the need is for a switching value rather than a holding value.



DUT = Device Under Test
CT = DC probe or equivalent
TG = Test generator with specified characteristics switching DUT to a specified on-state current, I_T, and then reducing the current at a specified di/dt to cause switch-off.
R = Resistor to define source resistance (if required)
CRO = Dual Channel Oscilloscope or equivalent

Figure 20—Test circuit for holding current (I_H)

When an impulse generator is used as the test generator, its output voltage may be too low at the holding current level for adequate discrimination of the switch off point. To increase the switch off voltage level, the generator and a current (< minimum specified value of I_H) from a dc voltage supply (<V_{DRM}) should be diode ORed on to the DUT (see Figure 21). Each switching quadrant of the thyristor SPD shall be separately tested and measured.

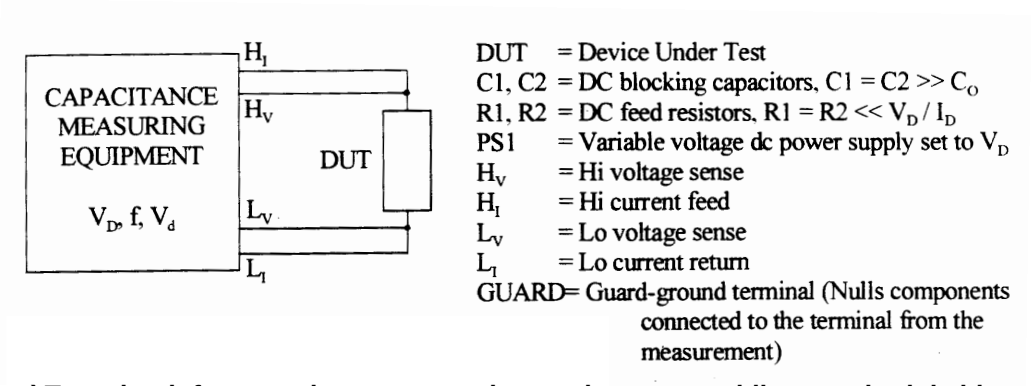


DUT = Device Under Test
CT = DC probe or equivalent
SG = Impulse generator with specified characteristics
PS = DC voltage power supply, set to specified voltage
R = Resistor to define dc
D1 = Isolating diode for PS
D2 = Isolating diode for SG
CRO = Dual Channel Oscilloscope or equivalent

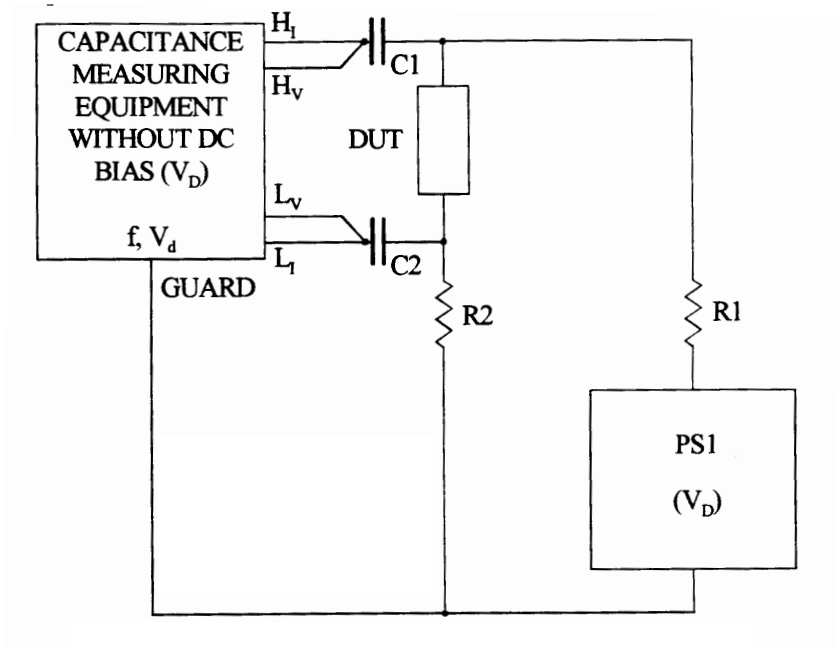
Figure 21—Test circuit for holding current with additional dc bias (impulse reset)

4.5.7 Off-state capacitance— C_O

The purpose of this test is to determine the off-state capacitance of a thyristor SPD under specified conditions. The test circuit used shall be functionally equivalent to Figure 22. The DUT off-state capacitance, C_O, shall be measured at specified dc (V_D) and ac (V_d and f) bias levels. In the absence of special requirements, it is recommended that an ac bias level of V_d = 0.1 Vrms at a frequency of 100 kHz < f, < 1 MHz be used. The dc bias level should be 0 V and any other levels that are representative of the intended application.



a) Test circuit for capacitance measuring equipment providing required dc bias



b) Test circuit for capacitance measuring equipment without dc bias capability

Figure 22—Test circuits a) and b) for capacitance (C_o)

Where a thyristor SPD has three terminals, the unmeasured terminal shall be nulled from the capacitance measurement and dc biased at levels that are representative of the intended application (see Figure 23). The same measurement technique may be used for multiple thyristor SPDs, which are packaged together and have four or more terminals, provided the nulled elements are directly between the measured and nulled terminals (see Figure 23); this measurement technique will not work if more than one of the nulled elements connect to an internal (non-terminal) node of the measured terminal pair.

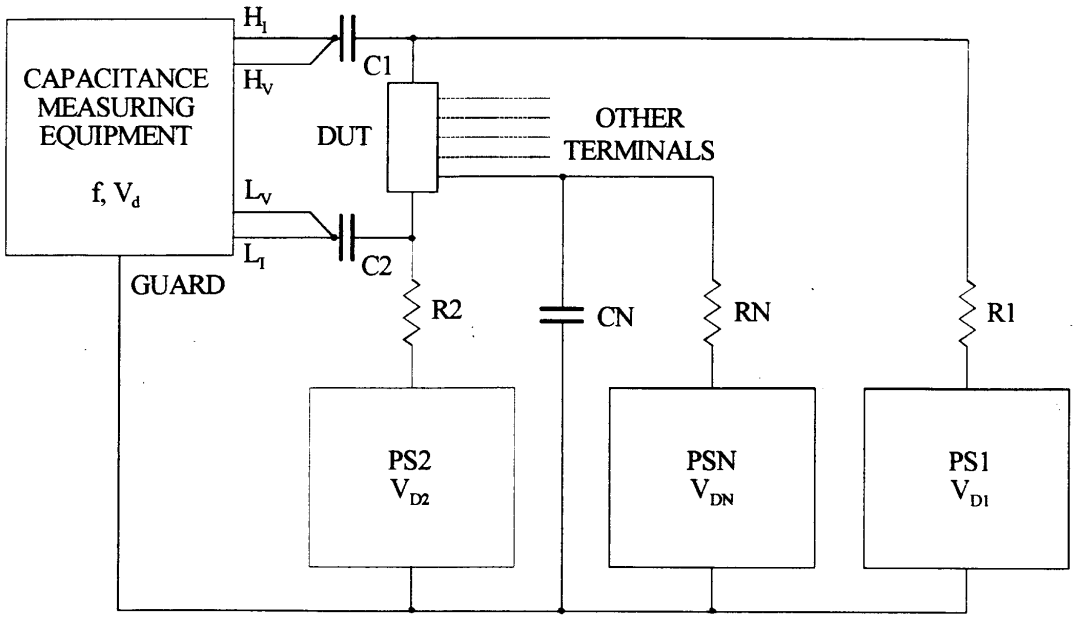
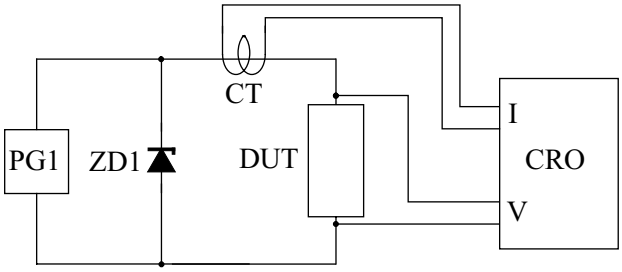


Figure 23—Test circuit for capacitance of a multi-device thyristor SPD

4.5.8 Breakdown voltage— $V_{(BR)}$

The purpose of this test is to determine the breakdown voltage of a thyristor SPD at a specified current level. A pulse of specified width and breakdown current, $I_{(BR)}$, amplitude shall be applied to the DUT and the stabilized value of breakdown voltage, $V_{(BR)}$, measured near the pulse end using a circuit functionally equivalent to Figure 24. In the absence of special requirements, it is recommended that the pulse width be less than 400 ms with a test current, $I_{(BR)}$, of 1 mA. Each switching polarity of the thyristor SPD shall be tested and measured separately. The value of $V_{(BR)}$ is junction temperature (initial and that due to testing) and test current dependent.

A positive breakdown slope thyristor SPD, Figures 1, 2, and 3, may have a low current portion of the breakdown characteristic where the breakdown voltage decreases for increasing current. By ramping the current from zero to the specified test current, $I_{(BR)}$, and measuring the DUT voltage with a peak-reading meter, the peak value of breakdown voltage, $V_{(BR)}M$, can be determined for the current range of zero to $I_{(BR)}$. The $V_{(BR)}M$ value can be used to determine the V_{DRM} rating if $I_{(BR)}$ is set to I_{DRM}. For a negative breakdown slope thyristor SPD (see Figures 4, 5, and 6) as this measurement approach can be used to determine $V_{(BO)}$.



DUT = Device under test
CT = DC current probe or equivalent
PG1 = Constant current pulse generator, $I_{(BR)}$
ZD1 = Voltage clamp > $V_{(BO)}$
CRO = Dual Channel Oscilloscope or equivalent

Figure 24—Test circuit for breakdown voltage ($V_{(BR)}$ at $I_{(BR)}$)

4.5.9 Switching voltage— V_S and current— I_S

The purpose of this test is to determine the switching point of a thyristor SPD at a specified ramp rate. The test circuit used shall be functionally equivalent to Figure 16. The test generator shall be specified for the open-circuit voltage and short-circuit current values, or equivalents, of rate-of-rise, wave shape, and wave shape peak value. The effective source impedance shall be greater than the maximum device switching resistance, R_S. The voltage and current waveforms as the DUT switches from off-state to on-state shall be recorded (see Figures 17–19). A V_I characteristic can be produced by plotting the recorded current against the recorded voltage. From this characteristic a visual estimate can be made of the switching point. Mathematically, a switching point occurs when the characteristic incremental slope impedance is the negative value of the source impedance. Finite source impedance values, heating, and switching time effects produce errors in determining the switching point, and switching voltage and current values should be used with caution. For gated thyristor SPDs, the switching voltage, V_S, may be approximated to the value of gate supply voltage, V_{GG}.

Each switching polarity of the thyristor SPD shall be separately tested and measured.

4.5.10 Forward voltage— V_F

The purpose of this test is to determine the forward voltage of a forward conducting thyristor SPD at a specified current; this voltage value is used to calculate the forward power loss. The test circuit and waveforms used shall be consistent with those used for the determination of on-state voltage, V_T (see Figure 16). The generator shall switch the DUT into forward conduction and the value of forward voltage, V_F, measured at a specified time or value of forward current, I_F. In the absence of special requirements, it is recommended that a time of 200 µs and a rectangular current impulse of 5 A be used for testing. Rapidly rising current waveforms may generate an additional forward recovery voltage; this should not be included in the V_F measurement (see Figure 25).

A low- and high-current value of V_F may be required to cover ac and impulse operation.

4.5.11 Peak forward recovery voltage— V_{FRM}

The purpose of this test is to determine the peak forward voltage of a forward conducting thyristor SPD under the condition of a fast rising current wavefront; this voltage value is the maximum stress on the protected circuitry. The test circuit and levels used shall be consistent with those used for the determination of fast impulse breakover voltage, $V_{(BO)}$ (see Figure 16). The generator shall switch the diode section on at a specified rate of forward current rise, dIF/dt, and the value of peak forward recovery voltage, V_{FRM}, shall be measured (see Figure 25). In the absence of special requirements, it is recommended that the fast impulse rate of rise shown in Table 2, 1000 V/µs and 10 A/µs, shall be used for testing.

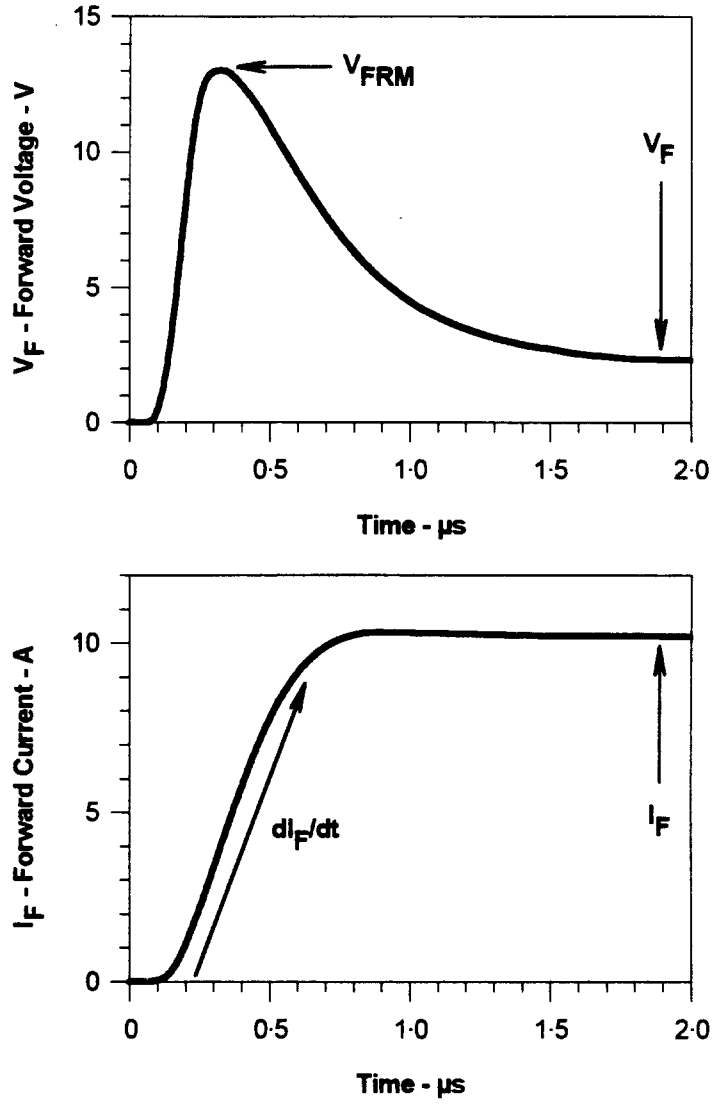


Figure 25—Diode peak forward recovery waveforms

4.5.12 Critical rate of rise of off-state voltage—*dv/dt*

The purpose of this test is to verify that the thyristor SPD will not turn on as a result of fast rising system voltages with peak amplitudes less than the V_{DRM} rating. A specified voltage ramp equal to the minimum value of critical dv/dt and of amplitude V_{DRM} shall be applied to the unenergized DUT. The peak ramp voltage shall be maintained for a period of at least 50 µs. The DUT shall not switch on, even partially, during the test. The voltage ramp can be of exponential or linear (see Figures 26 and 27). For an exponential ramp, the *dv/dt* value is calculated as $0.632V_{DRM}/t$

where

t is the time from the ramp start until the voltage rises to $0.632V_{DRM}$.

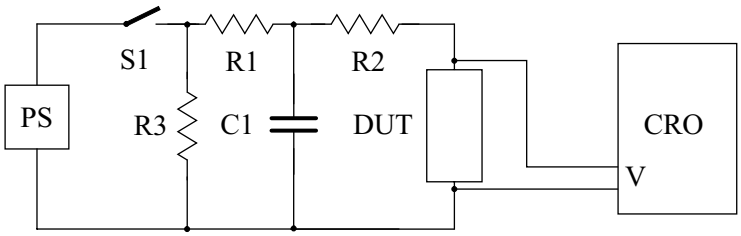
For a linear ramp, the *dv/dt* value is calculated as

$0.8V_{DRM}/(t_{90} - t_{10})$

where

t_{10} and t_{90} are the times at which the voltage has risen to $0.1V_{DRM}$ and $0.9V_{DRM}$, respectively.

Each switching polarity of the thyristor SPD shall be separately tested and measured.



DUT = Device under test
PS = DC voltage power supply
S1 = Start test switch
R1 = Charging Resistor
R2 = Current limit resistor if DUT switches
R3 = Discharge resistor after S1 opens
C1 = Charging capacitor
CRO = Oscilloscope or equivalent

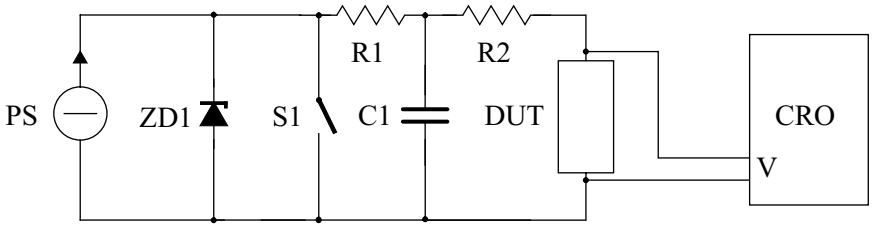
Figure 26—Test circuit for exponential critical rate of off-state voltage rise (*dv/dt*)

4.5.13 Impulse reset time— $t_{(RESET)}$

The purpose of this test is to verify that the thyristor SPD, having been switched into the on-state by a specified impulse, switches back to the off-state in the presence of a specified impulse reset current and within a specified duration. The thyristor SPD shall be tested in a circuit functionally equivalent to Figure 21. The value of direct current that flows when the device is replaced by a short circuit is called the impulse reset current. For a specified dc voltage, the value of resistor, *R* is adjusted to set the specified impulse rest current. The applied impulse shall be of the same polarity as the impulse reset current and specified for volt-

age and current wave shape and amplitude. It is recommended that the impulse reset time be measured from the virtual zero of the impulse to the time that the device switch-off voltage is 90% of the dc supply voltage.

In the absence of special requirements, each switching polarity of the thyristor SPD shall be separately tested and measured. In practice, the requirements of this test may be guaranteed by a correlated value of holding current.



DUT = Device under test
PS = Constant current supply, I
S1 = NC switch, opens to start test
R1 = Discharge resistor after S1 closes
R2 = Current limit resistor if DUT switches
C1 = Charging capacitor
ZD1 = Voltage Clamp at V_{DRM}
CRO = Oscilloscope or equivalent

Figure 27—Test circuit for linear critical rate of off-state voltage rise (*dv/dt*)

4.5.14 Temperature coefficient of breakdown voltage

The purpose of this test is to determine how the low current breakdown voltage, $V_{(BR)}$ of a thyristor SPD, varies with temperature as this represents a clipping level for circuit voltages. The value of $V_{(BR)}$ shall be measured over the specified operating temperature range. If the variation of $V_{(BR)}$ with temperature is non-linear it shall be expressed as a graph of voltage vs. temperature. If the variation of $V_{(BR)}$ with temperature is essentially linear it shall be expressed as either the average %/°C or mV/°C change over the specified temperature range.

$$\alpha_{V(BR)} = (V_{(BR)}T_{MAX} - V_{(BR)}T_{MIN})/(T_{MAX} - T_{MIN})\ \text{mV/°C}$$

or

$$= 100\ (V_{(BR)}T_{MAX} - V_{(BR)}T_{MIN})/[(T_{MAX} - T_{MIN})(V_{(BR)}T25)]\ \%/°C$$

where

T_{MAX} is the maximum operating temperature
T_{MIN} is the minimum operating temperature
T_{25} is the 25 °C reference temperature
$V_{(BR)TMAX} = V_{(BR)}$ at T_{MAX}
$V_{(BR)TMIN} = V_{(BR)}$ at T_{MIN}
$V_{(BR)T25} = V_{(BR)}$ at T_{25}

4.5.15 Variation of holding current with temperature

The purpose of this test is to determine how the holding current, I_H of a thyristor SPD, varies with temperature to ensure that the device will always switch off. The value of I_H (see 4.5.6) shall be measured over the specified operating temperature range and expressed as a graph of current vs. temperature.

4.5.16 Temperature derating

The purpose of this test is to verify the derating curve of a thyristor SPD to ensure reliable protector operation over the specified temperature range. Thyristor SPD ratings may derate at low as well as high temperatures. For V_{DRM}, V_{RM}, I_{FRM}, I_{FSM}, I_{PPS}, I_{TRM}, I_{TSM}, and di/dt, the relevant rating test procedures shall be used with the appropriate adjustment of stress level for the test temperature. Power derating can be verified by using the determined value of R_θ to calculate the maximum power for maximum junction temperature and a specified reference point temperature (ambient, case, or lead).

4.5.17 Thermal resistance— R_θ

The purpose of this test is to determine the continuous power capability of a thyristor SPD. The test circuit used shall be functionally equivalent to Figure 28. Immediately prior to the power being applied, the value of a temperature dependent characteristic shall be measured at the reference temperature. A constant value of power is then applied to the device. For short periods (<2% duty cycle) the power is interrupted to allow measurement of the temperature dependent characteristic. When these measurements stabilize, a steady-state condition has been reached. From a previous temperature characterization, the first and stabilized measurements can be converted to junction temperature values. If the stabilized junction temperature is not within +0% –20% of the device maximum junction temperature, T_{JM}, the test shall be continued with an appropriately adjusted power level until this is achieved. Expressing the measured values as a thermal resistance, R_θ, permits the calculation of the power capability at different reference and junction temperatures. The value of R_θ is calculated as

Thermal resistance, junction to ambient:

$$R_{\theta JA} = (T_{JPK}\text{-}T_A)/P_{TOT}\ ^\circ\text{C/W}$$

Thermal resistance, junction to case:

$$R_{\theta JC} = (T_{JPK}\text{-}T_C)/P_{TOT}\ ^\circ\text{C/W}$$

Thermal resistance, junction to lead:

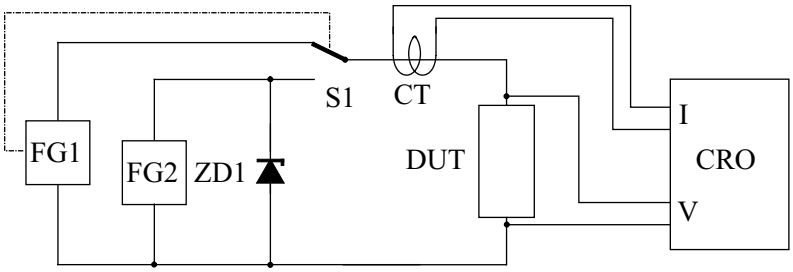
$$R_{\theta JD} = (T_{JPK}\text{-}T_L)/P_{TOT}\ ^\circ\text{C/W}$$

where

T_A is the ambient temperature reference
T_C is the case temperature reference, maintained at a constant value by cooling
T_L is the lead temperature reference, maintained at a constant value by cooling
T_{JPK} is the peak junction temperature, $0.8T_{JM} < T_{JPK} < T_{JM}$
P_{TOT} is the power pulse amplitude

Each switching and forward conducting polarity of the thyristor SPD shall be separately tested and measured. In the measurement period, it takes time to establish the measurement condition and read a value. During this time the junction temperature will be cooling and so the calculated temperature will be low. This

temperature error can be corrected by taking successive measurements after the power interruption and extrapolating the temperature decay back to the beginning of the interruption time.



DUT = Device under test
CT = DC current probe or equivalent
FG1 = Function generator for temperature sensitive characteristic measurement
FG2 = Constant power function generator
S1 = DUT switching between FG1 and FG2
ZD1 = Voltage clamp > $V_{(BO)}$
CRO = Dual Channel Oscilloscope or equivalent
- - - - - = FG1 and S1 synchronisation

Figure 28—Test circuit for thermal resistance and impedance

4.5.18 Transient thermal impedance— $Z_{\theta(t)}$

The purpose of this test is to determine the power capability of a thyristor SPD, for a specified power pulse duration, *t*. The test circuit used shall be functionally equivalent to Figure 28. Immediately prior to the power pulse, the value of a temperature dependent characteristic shall be measured at the reference temperature. The pulse of constant power is then applied for the specified duration. Immediately after the power pulse, the temperature dependent characteristic shall be remeasured. From a previous temperature characterization, these two measurements can be converted to junction temperature values. If the temperature after the power pulse is not within +0% -20% of the device maximum junction temperature, T_{JM}, the test shall be repeated with an appropriately adjusted power level until this is achieved. Adequate time shall be allowed between tests for the device to regain thermal equilibrium. Expressing the measured values as a thermal impedance, $Z_{\theta(t)}$, permits the calculation of the power capability at different reference and junction temperatures. The value of $Z_{\theta(t)}$ is calculated as:

Transient thermal impedance, junction to ambient for specified time interval (*t*)

$$Z_{\theta JA(t)} = (T_{JPK}\text{-}T_A)/P_{TOT}\ ^\circ\text{C/W}$$

Transient thermal impedance, junction to case for specified time interval (*t*)

$$Z_{\theta JC(t)} = (T_{JPK}\text{-}T_C)/P_{TOT}\ ^\circ\text{C/W}$$

Transient thermal impedance, junction to lead for specified time interval (*t*)

$$Z_{\theta JL(t)} = (T_{JPK}\text{-}T_C)/P_{TOT}\ ^\circ\text{C/W}$$

where

T_A is the ambient temperature reference

T_C is the case temperature reference, maintained at a constant value by cooling

T_L is the lead temperature reference, maintained at a constant value by cooling

T_{JPK} is the peak junction temperature, $0.8T_{JM} < T_{JPK} < T_{JM}$

P_{TOT} is the power pulse amplitude

t is the pulse width of power pulse

Each switching and forward conducting polarity of the thyristor SPD shall be separately tested and measured. After the power pulse, it takes time to establish the measurement condition and read a value. During this time, the junction temperature will be cooling and so the calculated temperature will be low. This temperature error can be corrected by taking successive measurements after the power pulse and extrapolating the temperature decay back to the time the pulse finished. In the absence of special requirements, it is recommended that the value of $Z_{\theta(t)}$ be determined over the range of 100 µs to a time duration approximating steady-state operation and expressed as a graph (see Figure 29).

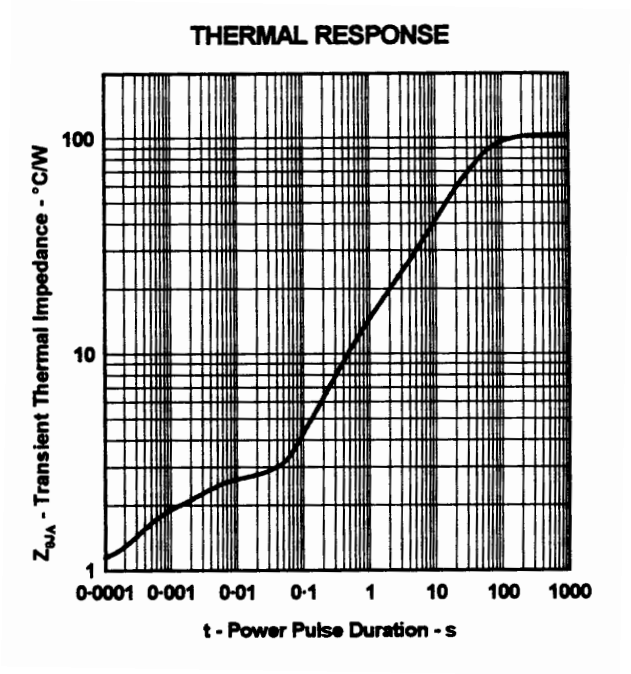
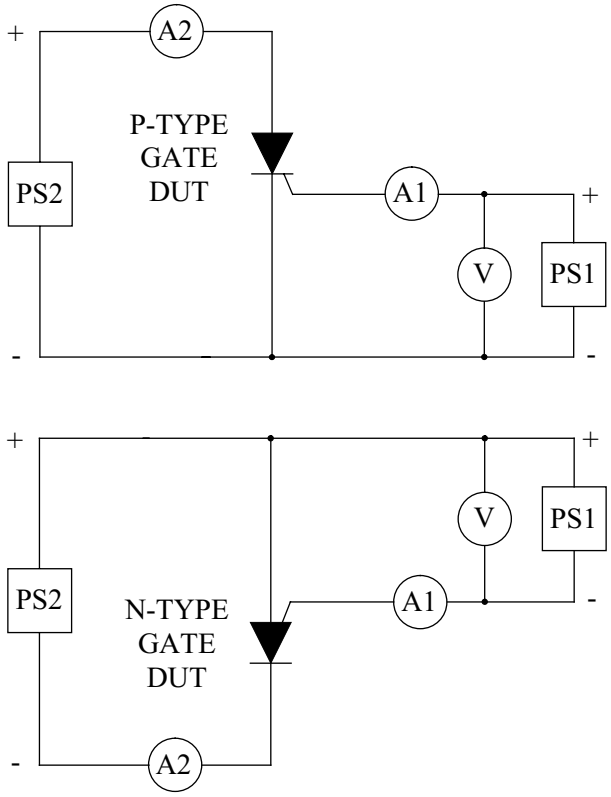


Figure 29—Thermal impedance vs. time

4.5.19 Gate-to-adjacent terminal peak off-state voltage and peak off-state gate current—V_{GDM}, I_{GDM}

The purpose of this test is to determine the maximum value of gate-to-adjacent terminal voltage of a thyristor SPD, that will maintain the protection terminals in a high impedance off-state condition at a specified voltage. Using the appropriate circuit of Figure 30, the specified value of V_D shall be impressed across the device protection terminals and the value of gate-to-adjacent terminal voltage increased from zero until the protection terminal current, I_D, reaches its specified value. The measured value of gate-to-adjacent terminal voltage is V_{GDM} and the measured gate current is I_{GDM}.

Each gated switching polarity of the thyristor SPD shall be separately tested and measured. The repetitive peak off-state voltage of a gated thyristor SPD is $V_{GG} + V_{GDM}$; this is equivalent to a fixed voltage thyristor SPD V_{DRM}.



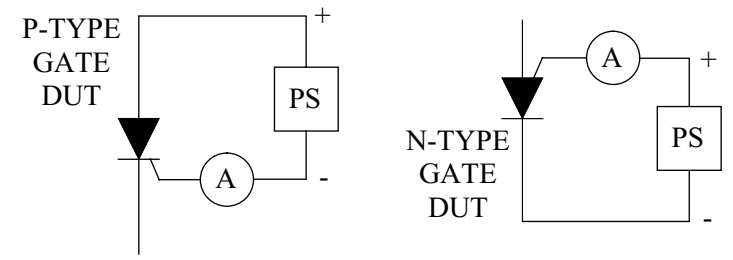
DUT = Device under test
A1 = Ammeter, measures gate current
A2 = Ammeter, I_D monitor
V = Voltmeter, measures gate to adjacent terminal voltage
PS1 = Variable dc voltage supply, set for a specified value of I_D
PS2 = DC voltage power supply, set to V_D

Figure 30—Test circuit for gate-to-adjacent terminal peak off-state voltage and current (V_{GDM} and I_{GDM})

4.5.20 Gate reverse current, adjacent terminal open—I_{GAO}, I_{GKO}

The purpose of this test is to determine the current drain on the gate terminal voltage supply when the adjacent terminal is open circuit. Using the appropriate circuit of Figure 31, the specified value of gate bias, V_{GG}, shall be applied to the gate and the current through the gate measured. This test determines the reverse gate to anode off-state current, I_{GAO}, of a p-gate device with the cathode terminal open or the reverse gate to cathode off-state current, I_{GKO}, of an n-gate device with the anode open.

Each gated switching polarity of the thyristor SPD shall be separately tested and measured.



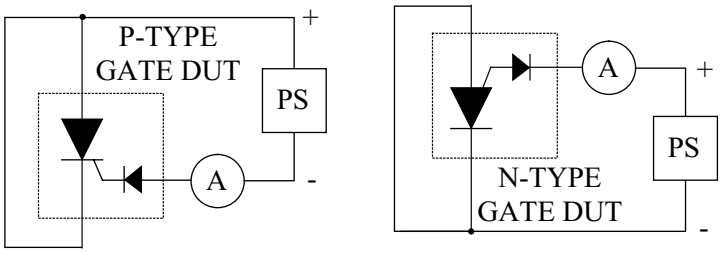
DUT = Device under test
A = Ammeter, for reverse gate current
PS = DC power supply, set at specified gate voltage, V_{GG}

Figure 31—Test circuit for gate reverse current, adjacent terminal open (I_{GAO}, I_{GKO})

4.5.21 Gate reverse current, main terminals short circuited— I_{GAS}, I_{GKS}

The purpose of this test is to determine the current drain on the gate terminal voltage supply when the adjacent terminal is shorted to the other protection terminal. Using the appropriate circuit of Figure 32, the specified value of gate bias, V_{GG}, shall be applied to the gate and the current through the gate measured. This test determines the reverse gate off-state current, I_{GAS}, of a p-gate device with the cathode shorted to the anode or the reverse gate off-state current, I_{GKS}, of an n-gate device with the anode shorted to the cathode.

Each gated switching polarity of the thyristor SPD shall be separately tested and measured. This test is specific to devices with integrated gate blocking diodes.



DUT = Device under test
A = Ammeter, for reverse gate current
PS = DC power supply, set at specified gate voltage, V_{GG}

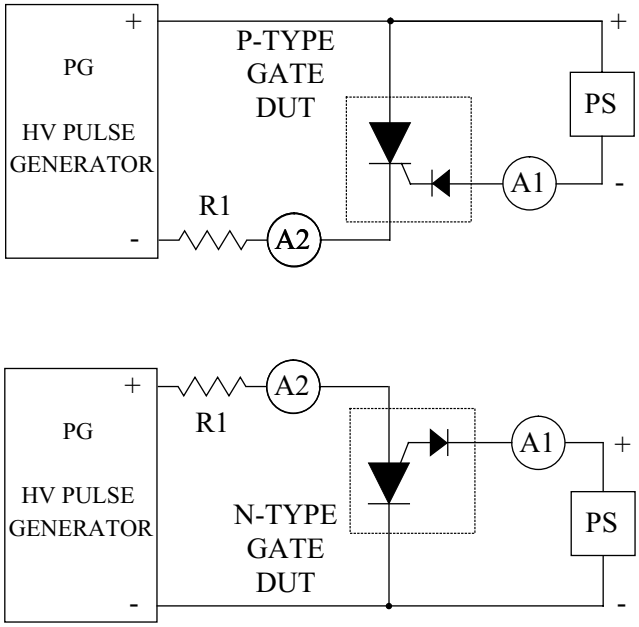
Figure 32—Test circuit for gate reverse current, main terminals short circuited (I_{GAS}, I_{GKS})

4.5.22 Gate reverse current, on-state—I_{GAT}, I_{GKT}

The purpose of this test is to determine the current drain on the gate terminal voltage supply when the thyristor SPD is in the on-state. Using the appropriate circuit of Figure 33, the specified value of gate bias voltage, V_{GG}, shall be applied to the gate and the device switched into the on-state by the generator connected across the protection terminals. The gate current shall be measured at the specified on-state

current, I_T. The generator and the value of I_T shall be the same as those used for the determination of the ac or dc value of V_T. This test determines the reverse gate current in the on-state, I_{GAT}, of a p-gate device or the reverse gate current in the on-state, I_{GKT}, of an n-gate device.

Each gated switching polarity of the thyristor SPD shall be separately tested and measured. This test shall only be used for devices with integrated gate blocking.



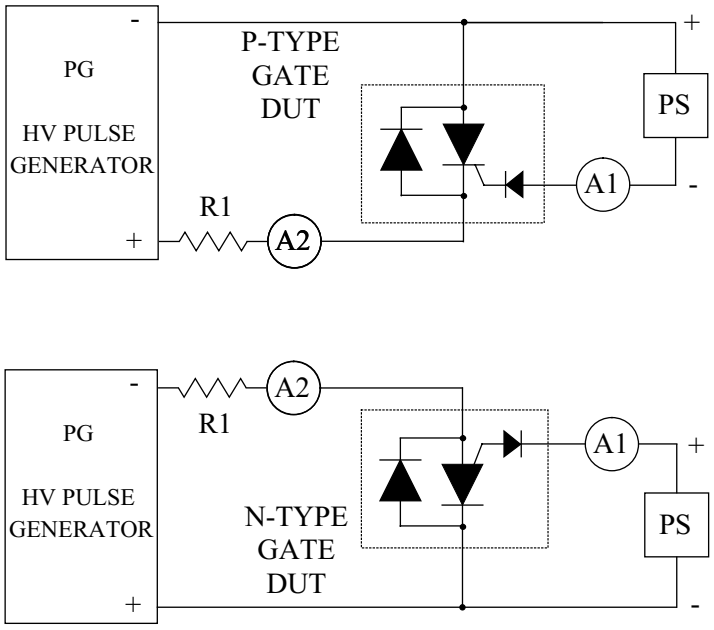
DUT = Device under test
A1 = Peak Current Meter, strobed to I_T
A2 = Peak Current Meter
PG = HV pulse generator with specified characteristics
PS = DC power supply, set at specified gate voltage, V_{GG}
R1 = Resistor, defines I_T

Figure 33—Test circuit for gate reverse current, on-state (I_{GAT}, I_{GKT})

4.5.23 Gate reverse current, forward conducting state—I_{GAF}, I_{GKF}

The purpose of this test is to determine the current drain on the gate terminal voltage supply when the forward conducting thyristor SPD is in diode conduction. Using the appropriate circuit of Figure 34, the specified value of gate bias voltage, V_{GG}, shall be applied to the gate and the device placed into the forward conducting state by the generator connected across the protection terminals. The gate current shall be measured at the specified forward conduction current, I_F. The generator and the value of I_F shall be the same as those used for the determination of the ac or dc value of V_F. This test determines the reverse gate current in the forward conducting state, I_{GAF}, of a p-gate device or the reverse gate current in the forward conducting state, I_{GKF}, of an n-gate device.

This test shall only be used for forward conducting thyristor SPDs with integrated gate blocking.



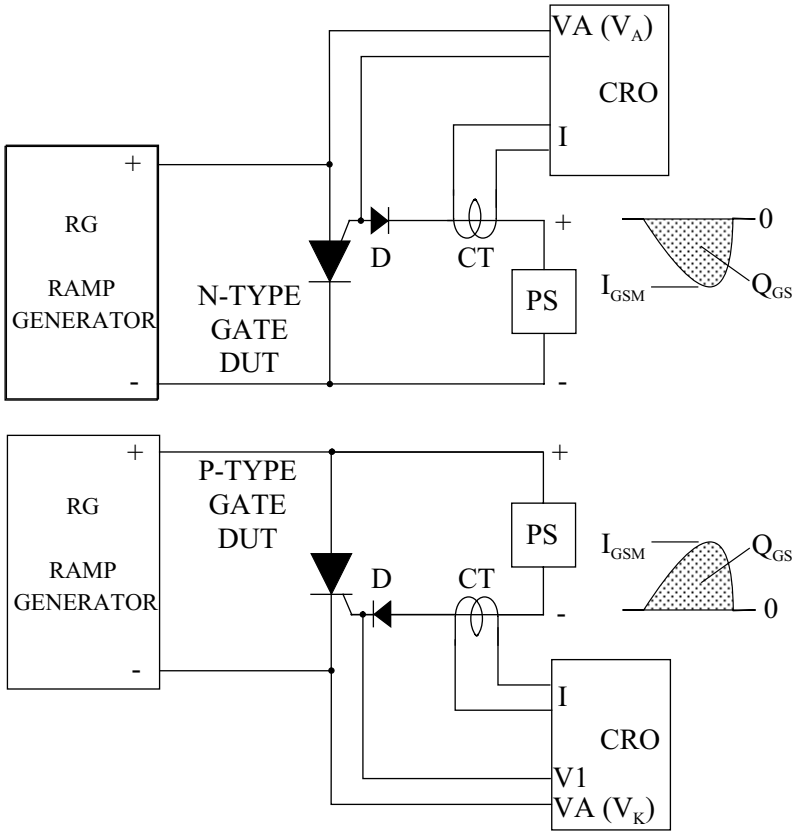
DUT = Device under test
A1 = Peak Current Meter, strobed to I_F
A2 = Peak Current Meter
PG = HV pulse generator with specified characteristics
PS = DC power supply, set at specified gate voltage, V_{GG}
R1 = Resistor, defines I_F

Figure 34—Test circuit for gate reverse current, forward conducting state (I_{GAF}, I_{GKF})

4.5.24 Gate switching charge—Q_{GS}

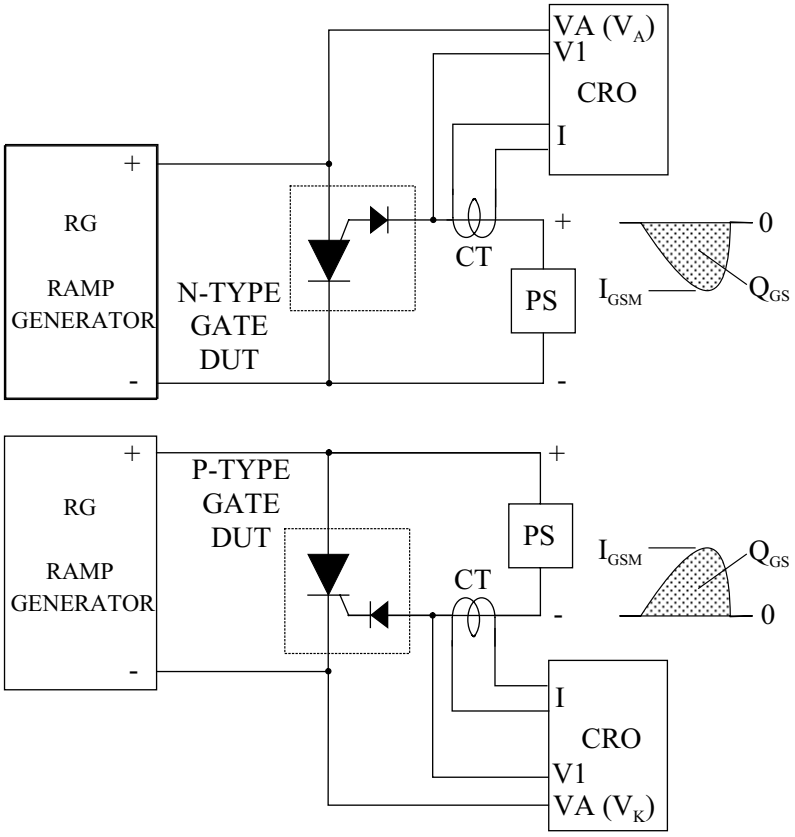
The purpose of this test is to determine the charge demand on the gate terminal supply, when the thyristor SPD is voltage limiting, to allow the dimensioning of the gate decoupling capacitor. Using the appropriate circuit of Figure 35 or 36, the specified value of gate bias voltage, V_{GG}, shall be applied to the gate and the device switched into the on-state by the generator connected across the protection terminals. The gate charge shall be measured by recording the gate current during the limiting period and integrating it (see example in Figure 37). The generator shall be the same as that used for the determination of the fast ramp rate $V_{(BO)}$.

Each gated switching polarity of the thyristor SPD shall be separately tested and measured.



DUT = Device Under Test
VA = Adjacent terminal voltage
V1 = Monitored gate voltage
D = Series gate diode
RG = Ramp generator with specified di/dt and dv/dt characteristics
PS = DC power supply, set at specified gate voltage, V_{GG}
CT = Current transformer or equivalent
CRO = Dual channel oscilloscpe or equivalent

Figure 35—Test circuit for gate switching current, gate switching charge, and gate-to-adjacent terminal breakover voltage (I_{GSM}, Q_{GS}, $V_{GK(BO)}$, $V_{GA(BO)}$)



DUT = Device Under Test
V_A = Adjacent terminal voltage
V1 = Monitored gate voltage
RG = Ramp generator with specified di/dt and dv/dt characteristics
PS = DC power supply, set at specified gate voltage
CT = Current transformer or equivalent
CRO = Dual channel oscilloscpe or equivalent

Figure 36—Test circuit of integrated gate diode DUT for gate switching current, gate switching charge and gate-to-adjacent terminal breakover voltage (I_{GSM}, Q_{GS}, $V_{GK(BO)}$, $V_{GA(BO)}$)

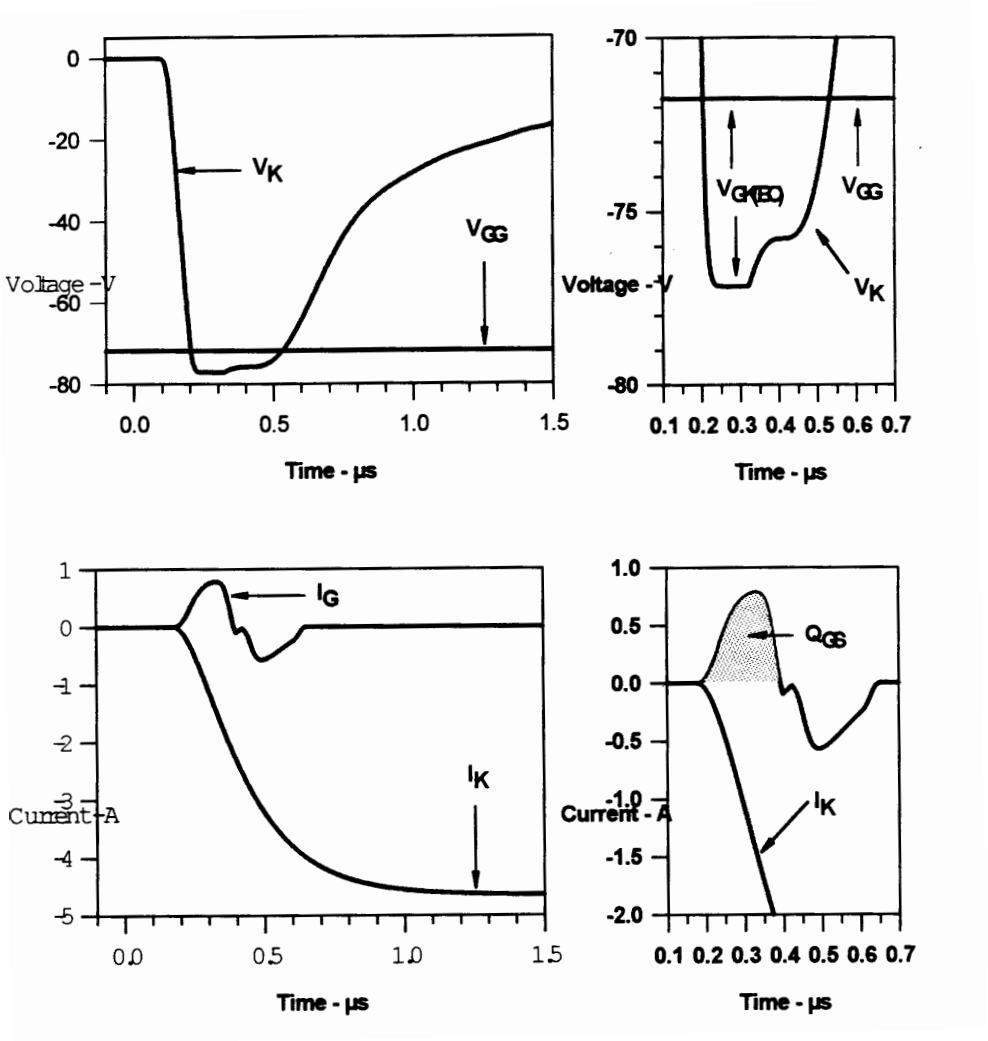


Figure 37—Overall and expanded clamping waveforms for a p-type gate DUT to illustrate $V_{GK(BO)}$ and Q_{GS} measurement (di_K/dt=10 A/µs)

4.5.25 Peak gate switching current— I_{GSM}

The purpose of this test is to determine the peak current demand on the gate terminal supply, when the thyristor SPD is voltage limiting, to provide design information for the gate supply so that excessive voltage rise does not occur. Using the appropriate circuit of either Figure 35 or 36, the specified value of gate bias voltage, V_{GG}, shall be applied to the gate and the device switched into the on-state by the generator connected across the protection terminals. The peak gate current, I_{GSM}, during the limiting period shall be measured. The generator shall be the same as that used for the determination of the slow ramp rate $V_{(BO)}$.

Each gated switching polarity of the thyristor SPD shall be separately tested and measured.

4.5.26 Gate-to-adjacent terminal breakover voltage—$V_{GK(BO)}$, $V_{GA(BO)}$

The purpose of this test is to determine the voltage difference between the gate supply and the breakover voltage of the thyristor SPD to allow calculation of the breakover voltage value over a range of supply voltages and ramp rates. Using the appropriate circuit of either Figure 35 or 36, the specified value of gate bias voltage, V_{GG}, shall be applied to the gate and the device switched into the on-state by the generator connected across the protection terminals. The peak value of gate-to-adjacent terminal voltage, at breakover, shall be measured (see example in Figure 37.) The generators shall be the same as those used for the determination of $V_{(BO)}$. This test determines the gate-to-cathode voltage at breakover, $V_{GK(BO)}$, of a p-gate device or the gate-to-anode voltage at breakover, $V_{GA(BO)}$, of an n-gate device.

Each gated switching polarity of the thyristor SPD shall be separately tested and measured.

5. Failure modes

In the absence of special requirements, the following criteria in subclauses 5.1 through 5.2 are suggested. Tests for determining failure shall be performed after the device temperature has returned to 25 ±5 °C.

5.1 Degradation failure mode

In this mode, a previously acceptable thyristor SPD exhibits a failure, which is gradual, partial, or both. The thyristor SPD exhibits a defined change in some characteristic. The device may still function satisfactorily in the application circuit.

NOTE— Such a failure does not cease all functions, but compromises a function. In time, such a failure may develop into a catastrophic failure. The characteristics most vulnerable to degradation are the reverse blocking and off-state voltage characteristics.

5.1.1 High off-state current failure mode

In this mode, the thyristor SPD has an off-state current of greater than a specified value.

NOTE—In the absence of requirements relating to special applications, the off-state current should be measured with the peak repetitive off-state voltage value applied.

5.1.2 High reverse current failure mode

In this mode, the thyristor SPD has a repetitive peak reverse current of greater than a specified value.

5.1.3 High breakover voltage failure mode

In this mode, the thyristor SPD has a breakover voltage of greater than a specified value.

5.1.4 Low holding current failure mode

In this mode, the thyristor SPD has a holding current lower than a specified value.

5.2 Catastrophic failure mode

In this mode, the thyristor SPD exhibits a sudden and complete change in characteristic that renders it inoperable. Catastrophic failure causes cessation of one or more fundamental functions of the thyristor SPD.

NOTE—This failure generally results in an electrical short between the main terminals. However, if the resulting short-circuit current is high enough, device internal parts may melt, and thus render the device open circuit.

5.2.1 Short-circuit failure mode

In this mode, the thyristor SPD has become permanently short-circuited.

NOTE—In the absence of requirements relating to special applications, the maximum value of impedance for a short circuit is determined as that value that will just prevent the protected equipment from normally functioning.

5.2.2 Open-circuit failure mode

In this mode, the thyristor SPD has become permanently open-circuit.

NOTE— In the absence of requirements relating to special applications, it is suggested, that in this mode, a failed device should not conduct more than the peak repetitive off-state current value when 150% of the maximum breakover voltage value is applied.

5.3 “Fail-safe” operation

The use of “fail-safe” to describe a failure mode of a thyristor SPD is to be discouraged for the following reason—failure of a device can occur in any of the modes described above. Some users may consider that the most desirable failure mode for the device is to maintain the protective function; for example, failure in the short-circuit failure mode. However, system objectives of other users can require that a particular device should fail in an open-circuit failure mode in order to achieve the desired performance of the system.

Thus, failure in the short mode, while considered “fail-safe” by many users, may in fact be opposite the desired “safe” mode of other users. Therefore, the recommended practice is to describe the failure by one of the failure modes defined in 5.1 through 5.2.

Annex A

(informative)

Thyristor terms

A.1 Definitions

The symbol (a) following a definition indicates that the definition is identical to that which appears in IEEE Std 100-1996 [B3]:

A.1.1 anode: The electrode by which current enters the thyristor, when the thyristor is in the on-state with the gate open-circuited.[a]

NOTE—This term does not apply to bi-directional thyristors.

A.1.2 bidirectional thyristor: A thyristor having substantially the same switching behavior in the first and third quadrants of the principal voltage-current characteristic.[a]

A.1.3 blocking: A term describing the state of a semiconductor device or junction that imposes high resistance to the passage of current.[a]

A.1.4 breakdown: A phenomena occurring in a reverse biased semiconductor junction, the initiation of which is observed as a transition from a region of high dynamic resistance to a region of substantially lower dynamic resistance for increasing magnitude of reverse current.

A.1.5 breakdown region: The portion of the characteristic that starts with the transition from the high dynamic resistance off-state to a substantially lower dynamic resistance and extending to the switching point.

A.1.6 breakover point: Any point on the principal voltage-current characteristic for which the differential resistance is zero and where the principal voltage reaches a maximum value.[a]

NOTE—For a thyristor SPD, the breakover point occurs in the breakdown region. If more than one breakover point exists in the breakdown region, the one with the highest voltage value shall be characterized.

A.1.7 cathode: The electrode by which current leaves the thyristor, when the thyristor is in the on-state with the gate open-circuited.[a]

NOTE—This term does not apply to bi-directional thyristors.

A.1.8 characteristic: An inherent and measurable property of a device. Such a property may be electrical, mechanical, thermal, hydraulic, electromagnetic, or nuclear, and can be expressed as a value for stated or recognized conditions. A characteristic may also be a set of related values, usually shown in graphical form.[a]

A.1.9 diode: A semiconductor device having two terminals and exhibiting a nonlinear voltage-current characteristic; in more-restricted usage, a semiconductor device that has the asymmetrical voltage-current characteristic exemplified by a single p-n junction.[a]

A.1.10 forward/reverse conducting quadrant: A quadrant of the principal voltage-current characteristic in which the device exhibits a forward direction conduction state. This will be quadrant 1 for a forward conducting thyristor SPD and quadrant 3 for a reverse conducting thyristor SPD.

A.1.11 forward-conducting diode thyristor surge protection device (SPD): A two-terminal internally triggered thyristor SPD that switches only for negative terminal-2 (cathode) voltage and conducts large currents at positive terminal-2 voltages comparable in magnitude to the on-state voltage.

NOTES

1—In conventional thyristor applications where the cathode is the common terminal, this device would be called a reverse-conducting diode thyristor.

2—When terminal 2 (cathode) is positive, the device characteristics are similar to those of a forward biased diode.

3—When terminal 2 (cathode) is negative, the device characteristics are similar to those of a breakover-triggered SCR.

A.1.12 forward-conducting triode thyristor surge protection device (SPD): A three-terminal thyristor SPD that switches only for negative main terminal-2 (cathode) voltage and conducts large currents at positive main terminal-2 voltages comparable in magnitude to the on-state voltage.

NOTES

1—In conventional thyristor applications where the cathode is the common terminal, this device would be called a reverse-conducting triode thyristor.

2—Application of an appropriate fixed gate voltage allows switching to take place at voltages well below the intrinsic breakover value.

3—When main terminal 2 (cathode) is positive, the device characteristics are similar to those of a forward biased diode.

A.1.13 forward direction: (1) The direction of current in a p-n junction that results when the p-type semiconductor region is at a positive potential relative to the n-type region. (2) The direction of current in a semiconductor device that results when the p-type semiconductor region connected to one terminal is at a positive potential relative to the n-type region connected to the other terminal.

NOTE—This definition does not apply if one or more junctions are connected in series with at least one other junction whose p and n regions are reversed.

A.1.14 gate: An electrode connected to one of the semiconductor regions to introduce a control current.

A.1.15 main terminals: The two terminals through which the principal current flows.

NOTE—The main terminals may be named by application usage. In telecommunications, terminals may be named after the line connections of R(ing), T(ip), and G(round) or A, B, and C(ommon).

A.1.16 main terminal 1: The main terminal that is named 1 by the device manufacturer.[a]

A.1.17 main terminal 2: The main terminal that is named 2 by the device manufacturer.[a]

A.1.18 maximum rating (absolute maximum rating): A rating that establishes either a limiting capability or a limiting condition beyond which damage to the device may occur.

NOTE—A limiting condition may be either a maximum or a minimum.

A.1.19 negative-breakdown resistance thyristor surge protection device (SPD): A thyristor SPD, whose static breakdown characteristic has a net negative-resistance slope prior to switching.

A.1.20 negative differential-resistance (region): The region of the principal voltage-current characteristic in the switching quadrant where the differential resistance is negative and the thyristor is switching between the breakdown and on-state regions.

A.1.21 n-gate thyristor: A three-terminal thyristor in which the gate terminal is connected to the n-region adjacent to the region to which the anode is connected and that is normally switched to the on state by applying a negative signal between the gate and anode terminals.

A.1.22 non-repetitive current rating: A maximum rating that may be applied to the device for a minimum of 100 times over the life of the device without failure. During the rated condition, the device is permitted to exceed its maximum rated junction temperature for short periods of time. The device is not required to block voltage or retain any gate control during or immediately following this rated condition until the device returned to the original thermal equilibrium conditions. This rated condition may be repeated after the device has returned to the original thermal equilibrium conditions.

A.1.23 off-state of a thyristor surge protection device (SPD): The state of a thyristor SPD, in a quadrant in which switching can occur, that corresponds to the high dynamic-resistance portion of the characteristic between the origin and the beginning of the breakdown region.

A.1.24 on-state (region): The condition of the thyristor corresponding to the low-resistance low-voltage portion of the principal voltage-current characteristic in the switching quadrant(s).

A.1.25 parameter: A device descriptor that is measurable or quantifiable, such as a characteristic or rating.

A.1.26 p-gate thyristor: A three-terminal thyristor in which the gate terminal is connected to the p-region adjacent to the region to which the cathode is connected and that is normally switched to the on state by applying a positive signal between the gate and cathode terminals.

A.1.27 positive-breakdown-resistance thyristor surge protection device (SPD): A thyristor SPD, whose static breakdown characteristic has a net positive-resistance slope prior to switching.

A.1.28 principal current: A generic term for the current through the device excluding any gate current.

NOTE—It is the current through both main terminals.

A.1.29 principal voltage: The voltage between the main terminals.

NOTES

1—In the case of reverse blocking and reverse conducting thyristors, the principal voltage is called positive when the anode potential is higher than the cathode potential, and called negative when the anode potential is lower than the cathode potential.

2—For bidirectional thyristors, the principal voltage is called positive when the potential of main terminal 2 is higher than the potential of main terminal 1.[a]

3—For forward-conducting thyristors the principal voltage is called positive when the cathode potential is higher than the anode potential, and called negative when the cathode potential is lower than the anode potential.

A.1.30 principal voltage-current characteristic: The function, usually represented graphically, relating the principal voltage to the principal current. Syn: principal characteristic.[a]

A.1.31 quadrant: When the principal voltage-current characteristic is expressed graphically, the voltage, v, and current, I, axes create four areas called quadrants. These quadrants are numbered counter clockwise as 1 through 4. The characteristic occurs in quadrant 1, +v and +i, and quadrant 3, -v and -i.

A.1.32 rating: The nominal value of any electrical, thermal, mechanical, or environmental quantity assigned to define the operating conditions under which a component, machine, apparatus, electronic device, etc., is expected to give satisfactory service.

NOTE—Rating is a generic term, but also see maximum rating.

A.1.33 repetitive rating: A maximum rating that may be continuously applied to the thyristor.

A.1.34 reverse-blocking diode thyristor surge protection device (SPD): A two-terminal thyristor SPD that exhibits a blocking state for positive cathode voltage.

A.1.35 reverse-blocking quadrant: Quadrant 3 of the principal voltage-current characteristic in which the device exhibits a reverse blocking state.

A.1.36 reverse-blocking triode thyristor surge protection device (SPD): A three-terminal thyristor SPD that exhibits a blocking state for positive cathode voltage.

A.1.37 reverse direction: (1) The direction of current in a p-n junction that results when the n-type semiconductor region is at a positive potential relative to the p-type region. (2) The direction of current in a semiconductor device that results when the n-type semiconductor region connected to one terminal is at a positive potential relative to the p-type region connected to the other terminal.

NOTE—This definition may not apply if one or more junctions are connected in series with at least one other junction whose p and n regions are reversed.

A.1.38 switching point: The point in the principal voltage-current characteristic which the thyristor regenerates and initiates switching into the on-state. This point occurs at the termination of the breakdown region and the start of the negative differential-resistance region.

A.1.39 switching quadrant: A quadrant of the principal voltage-current characteristic in which the device is intended to switch between the off-state and the on-state. For a bi-directional thyristor the switching quadrants will be 1 and 3. For a reverse blocking or reverse conducting thyristor the switching quadrant will be quadrant 1. For a forward conducting thyristor the switching quadrant will be quadrant 3.

A.1.40 thyristor: A bistable semiconductor device comprising three or more junctions that can be switched from the off-state to the on-state or vise versa, such switching occurring within at least one quadrant of the principal voltage-current characteristic.[a]

A.1.41 unidirectional thyristor surge protection device (SPD): A thyristor SPD that has switching characteristics in only quadrant.

NOTE—The main unidirectional thyristor SPDs are the reverse-blocking, reverse conducting and forward conducting thyristor SPDs.

A.2 General terms

A.2.1 clamping voltage: Peak voltage across the SPD measured under conditions of a specified peak pulse current and specified waveform.

NOTE—Peak voltage and peak current are not necessarily coincident in time.

A.2.2 crest (peak) value (of a wave, surge, or impulse): The maximum value that it attains.

A.2.3 impulse: A surge of unidirectional polarity.

A.2.4 impulse wave: A unidirectional wave of current or voltage of very short duration containing no appreciable oscillatory components.

NOTE—In the case of the 8/20 wave an opposite polarity wave tail underswing of up to 30% is allowed.

A.2.5 surge: A transient wave of current, potential or power in an electric circuit.

A.2.6 virtual duration of wavefront (of an impulse): The virtual value for the duration of the wavefront is as follows: (1) For voltage waves with wavefront duration less than 30 μs, either full or chopped on the front, crest, or tail, 1.67 times the time for the voltage to increase for 30% to 90% of its crest value. (2) For voltage waves with wavefront duration of 30 μs or more, the time taken by the voltage to increase from actual zero to maximum crest value. (3) For current waves, 1.25 times the time for the current to increase from 10% to 90% of crest value.

A.2.7 virtual zero point (of an impulse): The intersection with the zero axis of a straight line drawn through points on the front of the current wave at 10% and 90% crest value, or through points on the front of the voltage wave at 30% and 90% crest value.

A.2.8 wave: The variation with time of current, potential, or power at any point in an electric circuit.

A.2.9 waveform: A manifestation or representation (that is, graph, plot, oscilloscope presentation, equation(s), table of co-ordinate or statistical data, etcetera) or a visualization of a wave, pulse or transition.

A.2.10 wavefront (of a surge or impulse): That part which occurs prior to the crest value.

A.2.11 wave shape: The graph of the wave as a function of time.

A.2.12 wave shape designation (of an impulse): (1) The wave shape of an impulse (other than rectangular) of a current or voltage is designated by a combination of two numbers. The first, an index of the wavefront, is the virtual duration of the wavefront in microseconds. The second, an index of the wave tail, is the time in microseconds from virtual zero to the instant at which one-half of the crest value is reached on the wave tail. Examples are 1.2/50 and 8/20 waves. (2) The wave shape of a rectangular impulse of current or voltage is designated by two numbers. The first designates the minimum value of current or voltage that is sustained for the time in microseconds designated by the second number. An example is the 75 A 1000 μs wave.

A.2.13 wave tail (of an impulse): That part between the crest value and the end of the impulse.

Annex B

(informative)

Bibliography

[B1] IEC 61000-4-5: 1995, Electromagnetic compatibility (EMC) Part 4: Testing and measurement techniques—Section 5: Surge immunity test.

[B2] IEEE Std 4-1995, IEEE Standard Techniques for High-Voltage Testing (ANSI).

[B3] IEEE Std 100-1996, IEEE Standard Dictionary of Electrical and Electronics (ANSI).

[B4] IEEE Std C62.1-1989 (Reaff 1994), IEEE Standard for Gapped Silicon-Carbide Surge Arresters for AC Power Circuits (ANSI).

[B5] IEEE Std C62.33-1982 (Reaff 1994), IEEE Standard Test Specifications for Varistor Surge-Protective Devices (ANSI).

[B6] IEEE Std C62.35-1987 (Reaff 1993), IEEE Standard Test Specifications for Avalanche Junction Semiconductor Surge-Protective Devices (ANSI).